# Dual Ultra-Low On-Resistance Load Switch with Controlled Turn-On

## Features

- Integrated Dual Channel Load Switch
- Input Voltage Range: 0.8V to 5.5V
- Bias Input Supports: 2.5V to 5.5V
- Ultra-low Ron Resistance 19mΩ per channel
- 6A Continuous Switch Current per channel
- Low Quiescent Current
  - 32μA (Both Channel)
  - 26μA (Single Channel)
- Dual Separate Control Inputs
- Adjustable Slew-rate Control
- Quick Output Discharge Transistor
- Over Temperature Protection
- 14 Pin TDFN Package with Thermal Pad

## General Description

The P1498 is dual N-channel MOSFET power switch designed for high-side load-switching application. The device has a typical $R_{DS(ON)}$ of 19mΩ and the output current is limited to 6A. Each channel is controlled by an on/off input (EN1, EN2) independently, which is suitable for interfacing directly with low-voltage I/O ports.

In the P1498, a 200Ω on-chip load resistor is added for quick output discharge when the switch is turned off. Moreover, the controlled rise time can be adjusted by using a ceramic capacitor on the CTx pins in order to prevent in-rush current at start-up time.

The P1498 is available in 14 pin TDFN package.

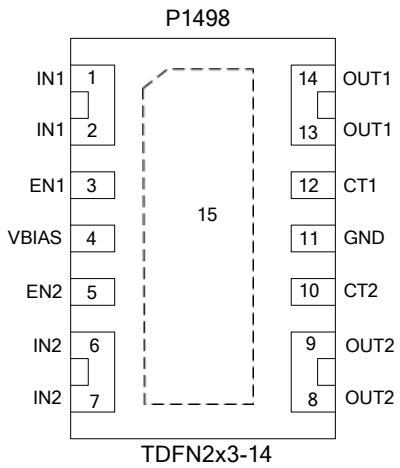
## Applications

- Notebooks / Netbooks
- Tablet PCs
- Consumer Electronics
- Set-Top-Boxes
- Industrial Systems
- Telecom Systems

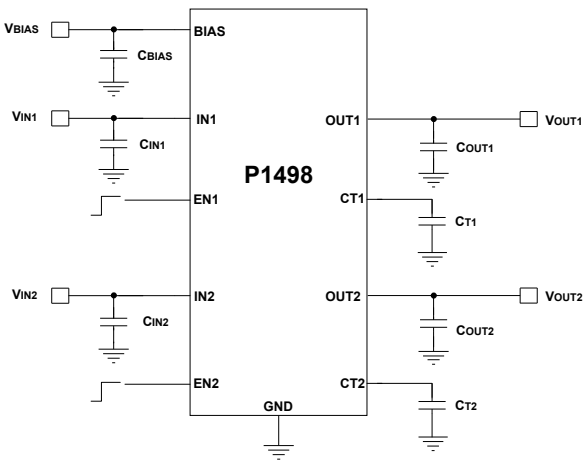
## Ordering Information

| ORDER NUMBER | MARKING | PACKAGE (Green) | Q'TY/BY REEL |
|---|---|---|---|
| P1498 | 98P | TDFN2X3-14 | 3000 / Tape & Reel |

## Pin Configuration



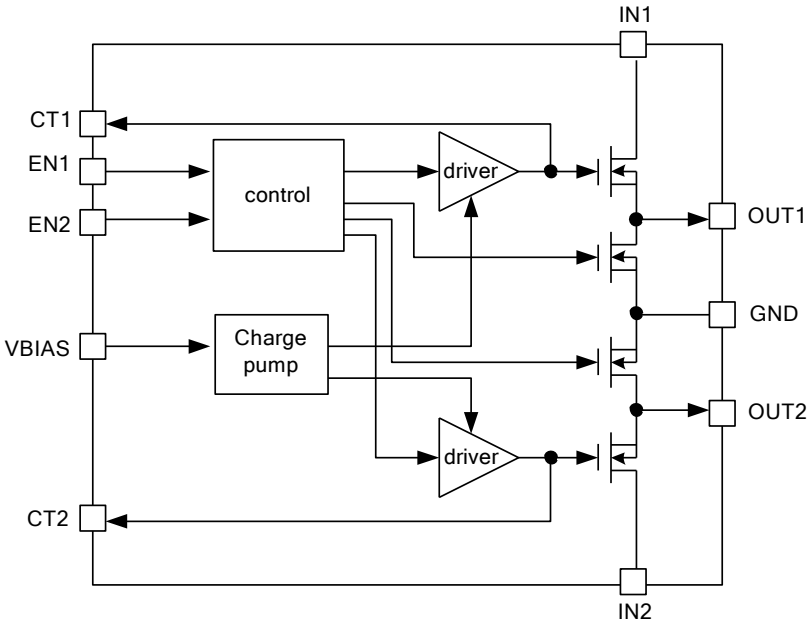

## Typical Application Circuit



## Pin Description

| PIN NO. | PIN NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | IN1 | I | Switch1 Input |
| 2 | IN1 | I | Switch1 Input |
| 3 | EN1 | I | Switch1 Control Input. Logic high turns on switch1. The EN1 pin cannot be left floating. |
| 4 | VBIAS | I | Input Bias Supply |
| 5 | EN2 | I | Switch2 Control Input. Logic high turns on switch2. The EN2 pin cannot be left floating. |
| 6 | IN2 | I | Switch2 Input |
| 7 | IN2 | I | Switch2 Input |
| 8 | OUT2 | O | Switch2 Output |
| 9 | OUT2 | O | Switch2 Output |
| 10 | CT2 | O | Switch2 Ramp capacitor input |
| 11 | GND | - | Ground |
| 12 | CT1 | O | Switch1 Ramp capacitor input |
| 13 | OUT1 | O | Switch1 Output |
| 14 | OUT1 | O | Switch1 Output |
| 15 | Thermal Pad | O | Exposed Pad to alleviate thermal stress. Solder to GND in PCB layout. |

## Block Diagram



## Absolute Maximum Ratings

$V_{IN1}$ ,$V_{IN2}$to GND . . . . . -0.3V to +6V
EN1,EN2 to GND . . . . . .-0.3V to +6V
$V_{OUT1}$ , $V_{OUT1}$to GND . . . . . -0.3V to +6V
CT1,CT2 to GND . . . . . .-0.3V to +12V
$V_{BIAS}$ to GND . . . . . -0.3V to +6V
Continuous Switch Current ($I_{MAX}$). . . . . 6A
Junction Temperature . . . . . .150°C
Thermal Resistance Junction to Ambient, ($\theta_{JA}$)*
TDFN2X3-14 . . . . . .69°C/W

Continuous Power Dissipation ($T_A$ = +25°C)*
TDFN2X3-14 . . . . . 1.9W
Thermal Resistance Junction to Case, ($\theta_{JC}$)
TDFN2X3-14 . . . . . .45°C/W
Operating Temperature Range . . . . . -40°C to 85°C
Storage Temperature Range . . . . . .-65°C to 150°C
Reflow Temperature (soldering, 10sec) . . . . . .260°C
ESD(HBM) . . . . . ±2KV(1)
ESD(CDM) . . . . . ±500V

*Please refer to Minimum Footprint PCB Layout Section
Note 1：Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

## Recommended Operating Conditions

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input voltage range | $V_{IN1,2}$ | 0.8 | | $V_{BIAS}$ | V |
| Bias voltage range | $V_{BIAS}$ | 2.5 | | 5.5 | V |
| VOUT Output Current (Single Channel) | $I_{OUT}$ | 0 | | 6 | A |
| Maximum Pulsed Switch Current, Pulse<300μs,1% Duty Cycle (Single Channel) | | | 8 | | A |
| ON voltage range | EN1,2 | 0 | | 5.5 | V |
| Output voltage range | $V_{OUT1,2}$ | | | VIN1,2 | V |
| High-level input voltage, EN1, EN2 | $V_{IH}$ | 1.2 | | 5.5 | V |
| Low-level input voltage, EN1, EN2 | $V_{IL}$ | | | 0.5 | V |
| Input Capacitor | $C_{IN1,2}$ | 1* | | | μF |

*Note: 1uF input capacitor is sufficient in most application cases. If the distance of power trace on PCB is longer than general design, larger input capacitor is highly recommended for normal operation.

## Electrical Characteristics

**($V_{IN1}$ = 0.8V to 5.5V, $V_{IN2}$ = 0.8V to 5.5V, $V_{BIAS}$= 5V, $T_A$ = 25ºC (unless otherwise noted)**

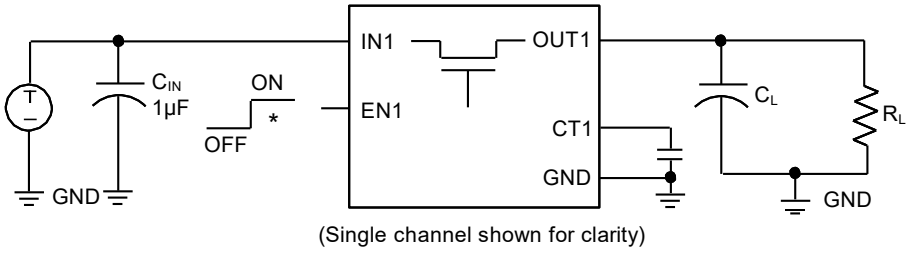
| PARAMETER | SYMBOL | Conditions | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | | 0.8 | | $V_{BIAS}$ | V |
| Bias Voltage Range | $V_{BIAS}$ | | | 2.5 | | 5.5 | V |
| Bias Current | $I_{BIAS}$ | IOUT1 = IOUT2 = 0,<br>VIN1 = VIN2 = 5V<br>EN1 = EN2 = $V_{BIAS}$ = 5V | | | 32 | 55 | μA |
| | | IOUT1 = IOUT2 = 0,<br>VIN1 = VIN2 = 5V<br>EN1 = $V_{BIAS}$ = 5V, EN2 = 0V | | | 26 | 45 | μA |
| | | IOUT1 = IOUT2 = 0,<br>VIN1 = VIN2 = 2.5V<br>EN1 = EN2 = $V_{BIAS}$ = 2.5V | | | 32 | 55 | μA |
| | | IOUT1 = IOUT2 = 0,<br>VIN1 = VIN2 =2.5V<br>EN1 = $V_{BIAS}$ = 2.5V, EN2 = 0V | | | 26 | 45 | μA |
| Shutdown Bias Current | $I_{SHDN}$ | ENx = GND, VOUTx = 0V | | | | 1 | μA |
| Off-state Supply Current | $I_{IN\_OFF}$ | ENx = GND, VOUTx = 0V,<br>VINx= 0.8 to 5V | | | | 1 | μA |
| EN pin Input leakage Current | $I_{EN\_LEAK}$ | EN=5.5V | | | | 1 | μA |
| On -Resistance | $R_{DS(on)}$ | ENx = $V_{BIAS}$,<br>IOUTx = -200mA<br>$V_{BIAS}$ = 5V, | VINx=5V | | 19 | 25 | mΩ |
| | | | VINx=3.6V | | 19 | 25 | |
| | | | VINx=1.8V | | 19 | 25 | |
| | | | VINx=0.8V | | 19 | 25 | |

## Electrical Characteristics (Continued)

**($V_{IN1}$ = 0.8V to 5.5V, $V_{IN2}$ = 0.8V to 5.5V, $V_{BIAS}$= 5V, $T_A$ = 25ºC (unless otherwise noted)**

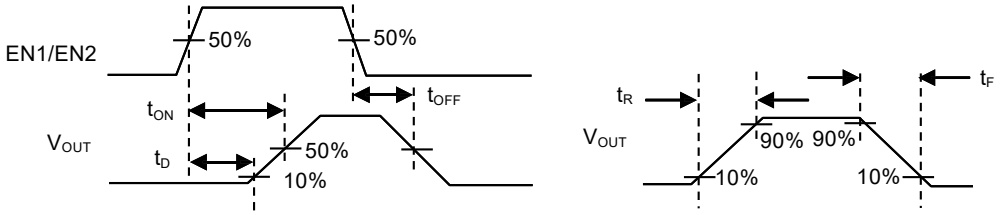
| PARAMETER | SYMBOL | Conditions | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| On -Resistance | $R_{DS(on)}$ | ENx =$V_{BIAS}$, IOUTx = -200mA $V_{BIAS}$ = 2.5V, | VINx=2.5V | | 19 | 25 | mΩ |
| | | | VINx=1.8V | | 19 | 25 | |
| | | | VINx=1.2V | | 19 | 25 | |
| | | | VINx=0.8V | | 19 | 25 | |
| Discharge Resistance | $R_{DIS}$ | VINx = 5.0V,ENx = 0V, IOUTx = 1mA | | | 200 | 300 | Ω |
| High level input voltage on EN pin | VIH | | | 1.2 | | 5.5 | V |
| Low level input voltage on EN pin | VIL | | | | | 0.5 | V |
| Over Temperature Threshold | TOTP | | | | 150 | | ºC |
| Over Temperature Hysteresis | THYS | | | | 20 | | ºC |

## Parametric Measurement Information




(Single channel shown for clarity)

**Test Circuit**




**$t_{ON}$ / $t_{OFF}$ WAVEFORMS**

*. Rising and falling time of control signal EN1,EN2 is 100ns

**Figure 1. Test Circuit and $t_{ON}$ / $t_{OFF}$ Waveforms**

## SWITCHING CHARATERISTICS

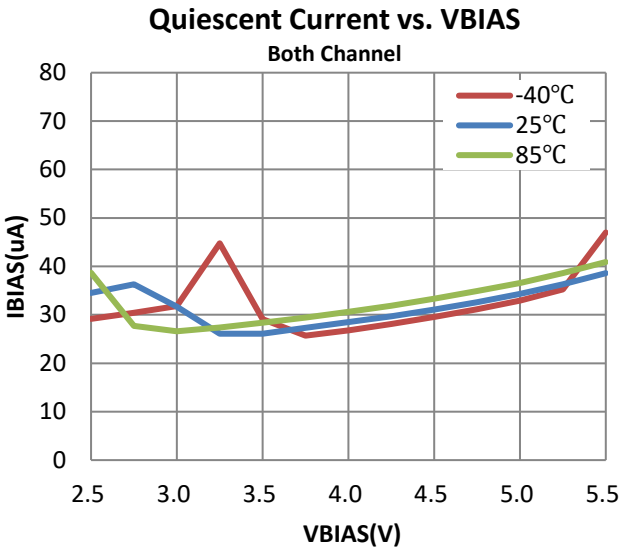
| PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **$V_{IN}$=$V_{EN}$=$V_{BIAS}$=5V, $T_A$=25ºC (unless otherwise noted)** | | | | | |
| $t_{ON}$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 1210 | | μs |
| $t_{OFF}$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 1 | | |
| $t_R$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 1600 | | |
| $t_F$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 2 | | |
| $t_D$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 420 | | |
| **$V_{IN}$=0.8V, $V_{EN}$=$V_{BIAS}$=5V, $T_A$=25ºC (unless otherwise noted)** | | | | | |
| $t_{ON}$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 440 | | μs |
| $t_{OFF}$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 1.2 | | |
| $t_R$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 315 | | |
| $t_F$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 2 | | |
| $t_D$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 280 | | |
| **$V_{IN}$=2.5V, $V_{EN}$=5V, $V_{BIAS}$=2.5V, $T_A$=25ºC (unless otherwise noted)** | | | | | |
| $t_{ON}$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 810 | | μs |
| $t_{OFF}$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 2.5 | | |
| $t_R$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 870 | | |
| $t_F$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 2 | | |
| $t_D$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 360 | | |
| **$V_{IN}$=0.8V, $V_{EN}$=5V, $V_{BIAS}$=2.5V, $T_A$=25ºC (unless otherwise noted)** | | | | | |
| $t_{ON}$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 480 | | μs |
| $t_{OFF}$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 3 | | |
| $t_R$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 330 | | |
| $t_F$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 2 | | |
| $t_D$ | $R_L$=10Ω, $C_L$=0.1μF, $C_T$=1000pF | | 300 | | |

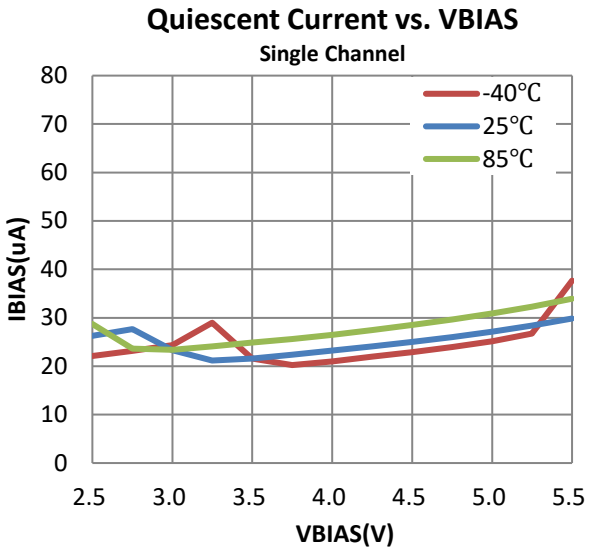
## Adjustable rise time

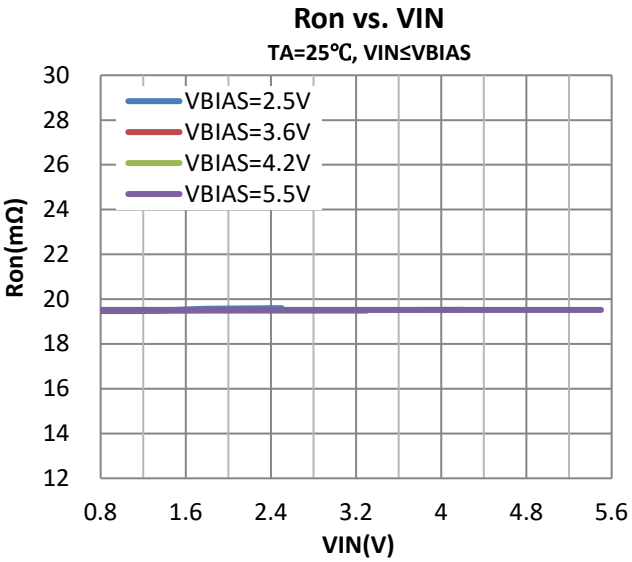
A capacitor to GND on the CT pins sets the slew rate for each channel. To ensure desired performance, a capacitor with a minimum voltage rating of 25V should be used on the CT pin.
Rise time can be calculated by multiplying the input voltage by the slew rate. The table below contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where $V_{IN}$ and $V_{BIAS}$ are already in steady state condition and the EN pin is asserted high.

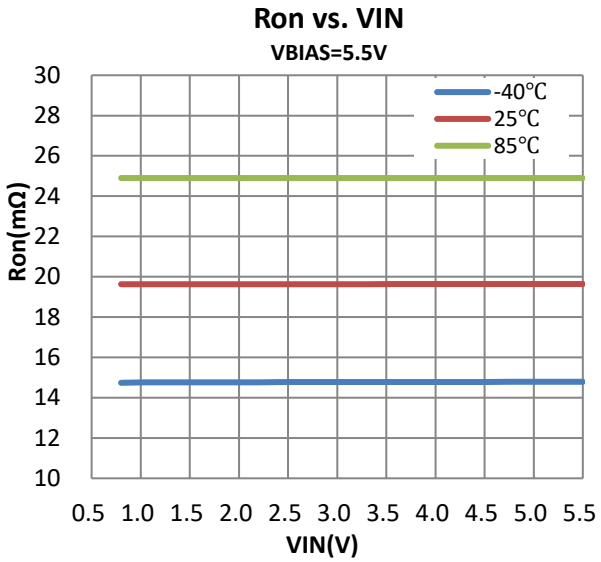
| CTx(pF) | Rise time (μs) 10% - 90%, $C_L$=0.1μF, $C_{IN}$=1μF, $R_L$=10Ω Typical values at 25ºC, $V_{BIAS}$=5V | | | | | | |
|---|---|---|---|---|---|---|---|
| | 5V | 3.3V | 1.8V | 1.5V | 1.2V | 1.05V | 0.8V |
| 0 | 145 | 120 | 78 | 70 | 62 | 56 | 46 |
| 220 | 426 | 290 | 191 | 170 | 142 | 138 | 115 |
| 470 | 820 | 556 | 328 | 298 | 246 | 220 | 177 |
| 1000 | 1550 | 1048 | 590 | 496 | 422 | 398 | 328 |
| 2200 | 2950 | 1859 | 1037 | 890 | 726 | 630 | 526 |
| 4700 | 6995 | 4640 | 2440 | 2200 | 1760 | 1490 | 1220 |
| 10000 | 16040 | 10450 | 5860 | 4760 | 3980 | 3510 | 2730 |

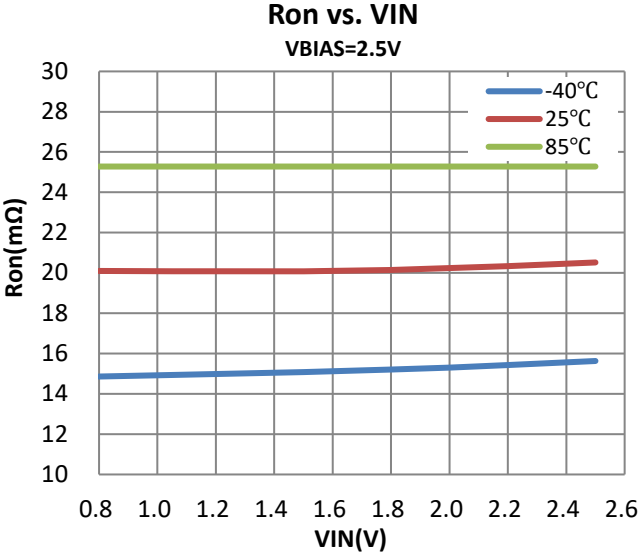
## Typical Performance Characteristics

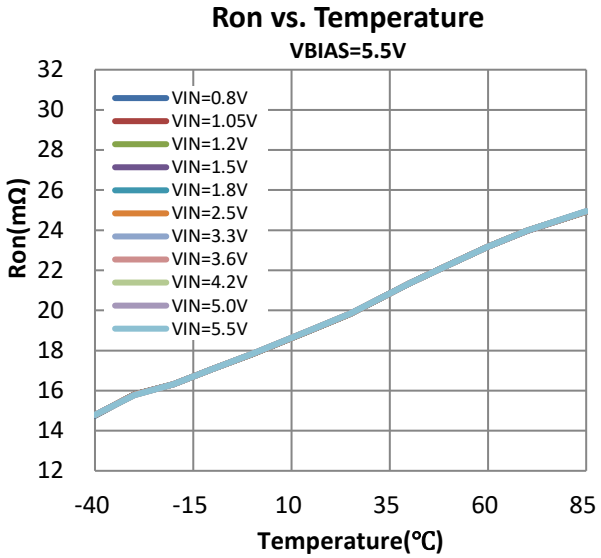


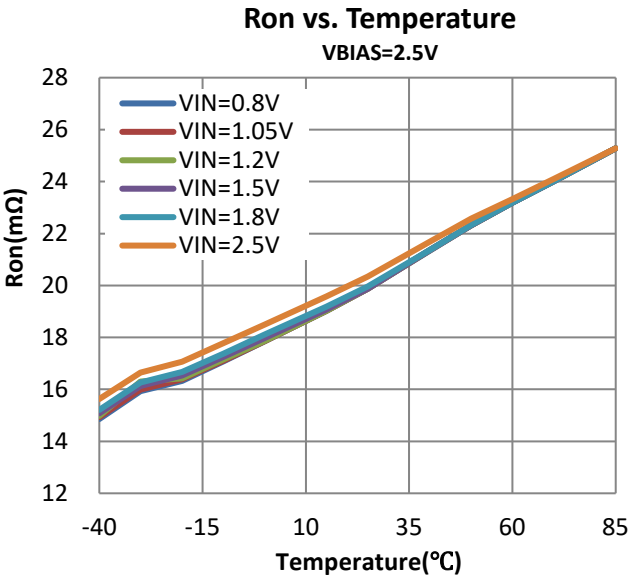



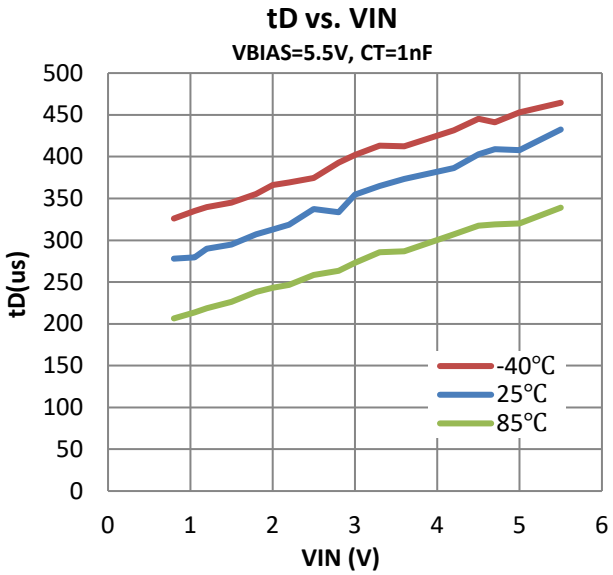



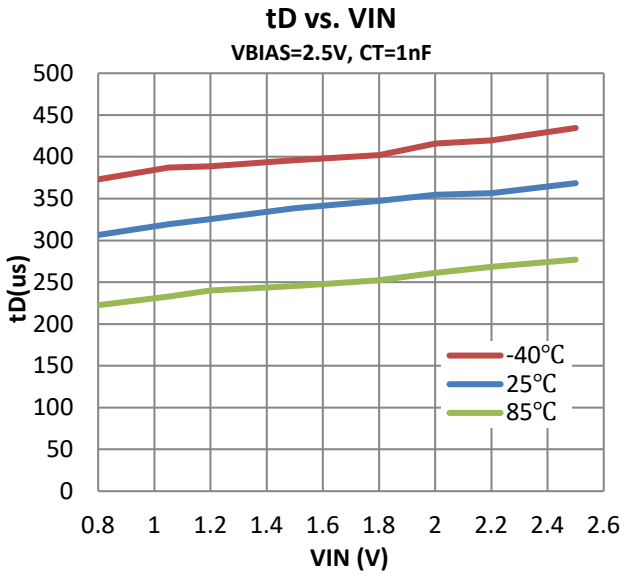



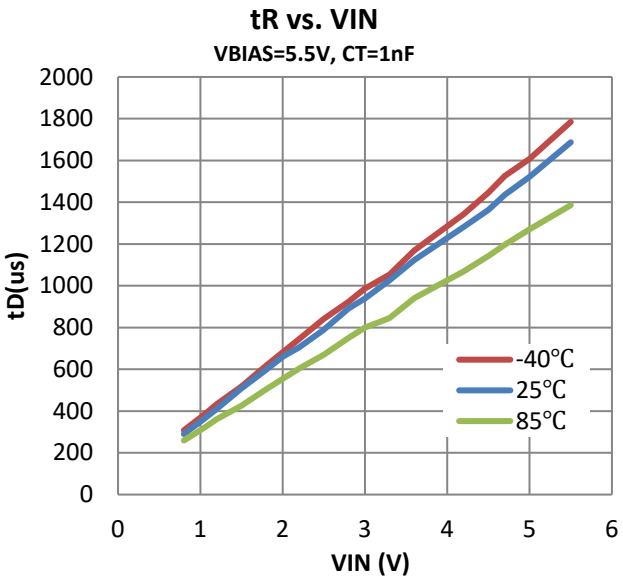



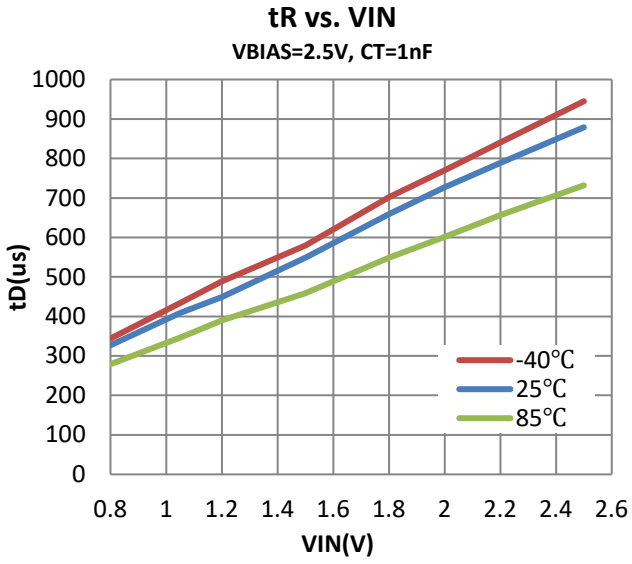
## Typical Performance Characteristics



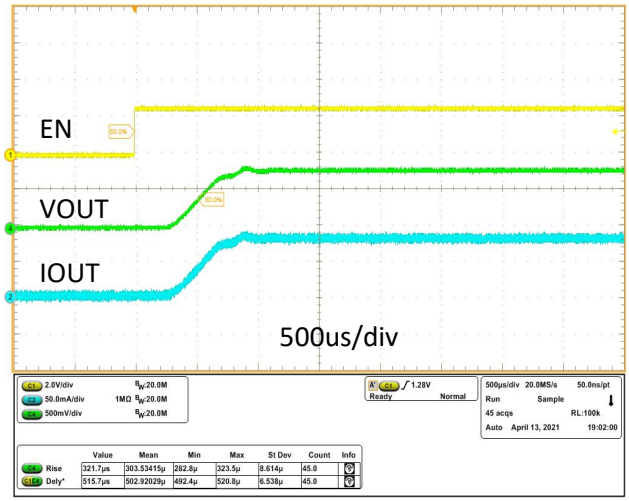



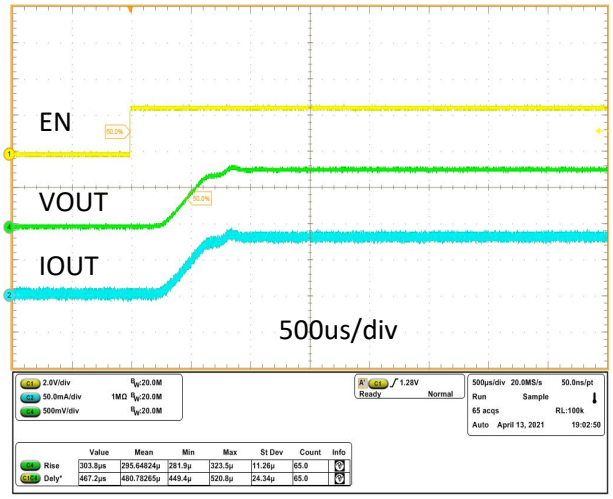



## Typical Performance Characteristics

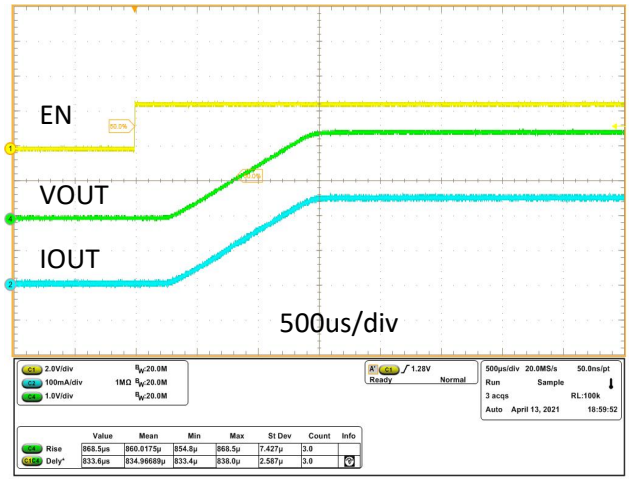
### Turn On Response Time
(VIN=0.8V,VBIAS=2.5V, CT=1nF,RL=10Ω)



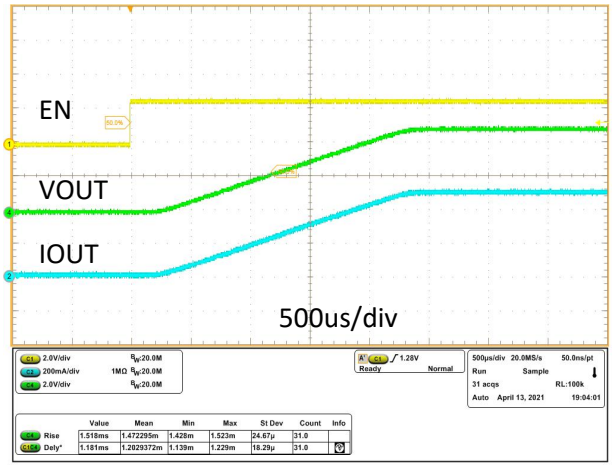

### Turn On Response Time
(VIN=0.8V,VBIAS=5.0V,CT=1nF,RL=10Ω)



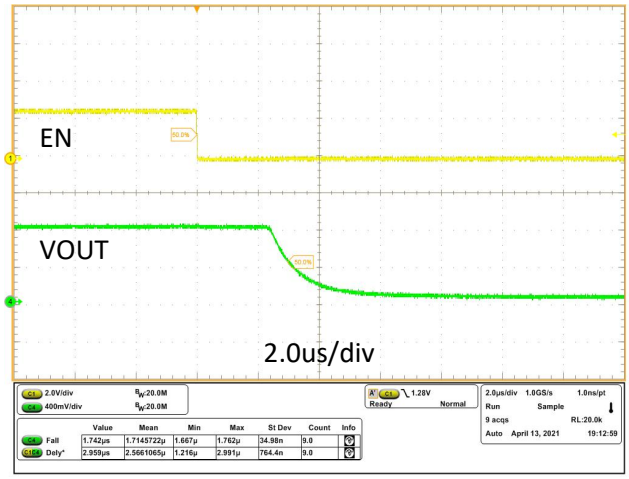

### Turn On Response Time
(VIN=2.5V,VBIAS=2.5V, CT=1nF,RL=10Ω)



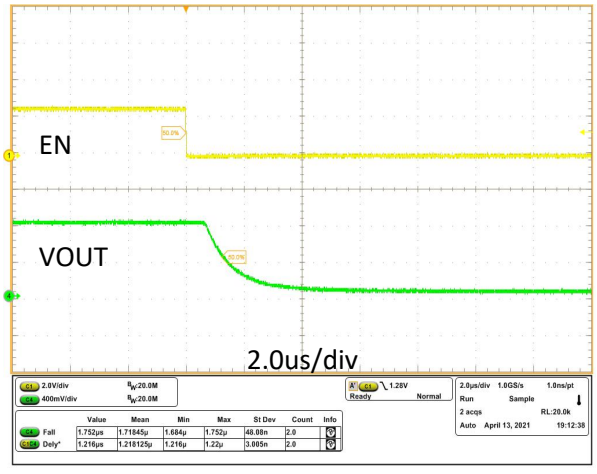

### Turn On Response Time
(VIN=5.0V,VBIAS=5.0V,CT=1nF,RL=10Ω)




### Turn Off Response Time
(VIN=0.8V,VBIAS=2.5V, CT=1nF,RL=10Ω)

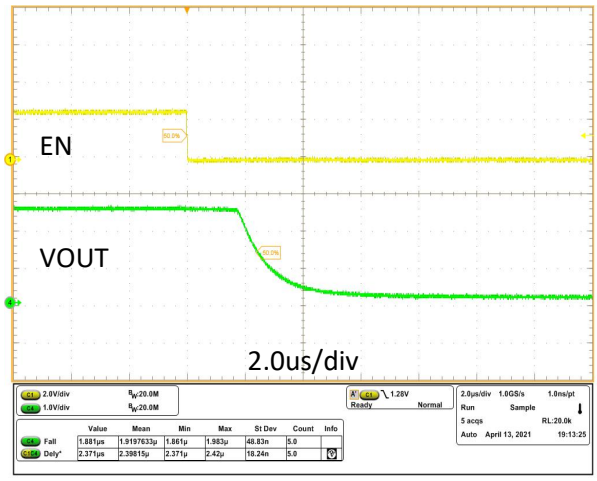



### Turn Off Response Time
(VIN=0.8V,VBIAS=5.0V,CT=1nF,RL=10Ω)

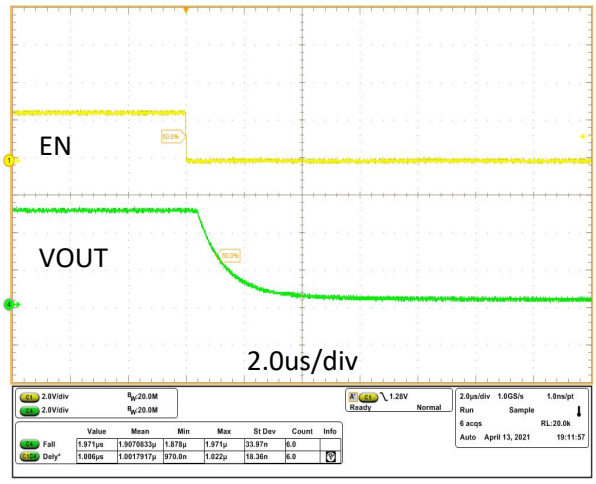


## Typical Performance Characteristics

**Turn Off Response Time**
**(VIN=2.5V,VBIAS=2.5V, CT=1nF,RL=10Ω)**




**Turn Off Response Time**
**(VIN=5.0V,VBIAS=5.0V,CT=1nF,RL=10Ω)**



## Application Information

### Enable Control

The P1498 is a dual channel MOSFET power switch. Each channel is controlled by an on/off input (EN1, EN2) independently. A logic high applies to this pin turns on the switch , and a logic low signal shuts down the output, as shown in the following table. The enable pin cannot be left floating.

| Logic of Enable Pin | | Status of Switch | |
|---|---|---|---|
| EN1 | EN2 | Switch1 | Switch2 |
| L | L | OFF | OFF |
| L | H | OFF | ON |
| H | L | ON | OFF |
| H | H | ON | ON |

### Input capacitor (optional)

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharge load capacitor or short-circuit, a capacitor need to be placed between $V_{IN}$ and GND. A 1μF ceramic capacitor, $C_{IN}$, placed close to the pins, is usually sufficient. Higher values of $C_{IN}$ can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommend- ed to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

### Output capacitor (optional)

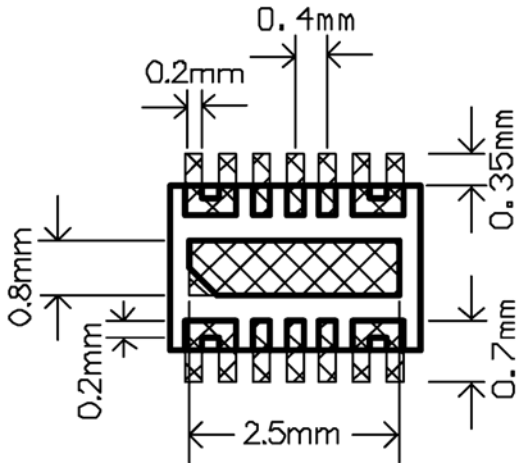
Due to the integrated body diode in the NMOS switch, a CIN greater than CL is highly recommended. A $C_L$ greater than $C_{IN}$ can cause $V_{OUT}$ to exceed $V_{IN}$ when the system supply is removed. This could result in current flow through the body diode from $V_{OUT}$ to $V_{IN}$. A $C_{IN}$ to $C_L$ ratio of 10 to 1 is recommended for minimizing $V_{IN}$ dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance in not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more $V_{IN}$ dip upon turn due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time.

## PCB Layout Guidelines

1. To have lower voltage drop in field application, short and wide PCB trace is recommended. The IN/OUT pins are located in corner of IC. It is beneficial to route a wide and short PCB trace.
2. To absorb voltage bounce that is caused by parasitic inductor of PCB trace at quick load transient, placing Cin /Cout close to IN/OUT pin of IC is recommended.
3. The wide trace of Vin/VOUT and GND can help minimize the parasitic electrical effects and the case to ambient thermal impedance. Using thermal vias located under the exposed thermal pad helps thermal dissipation of the device

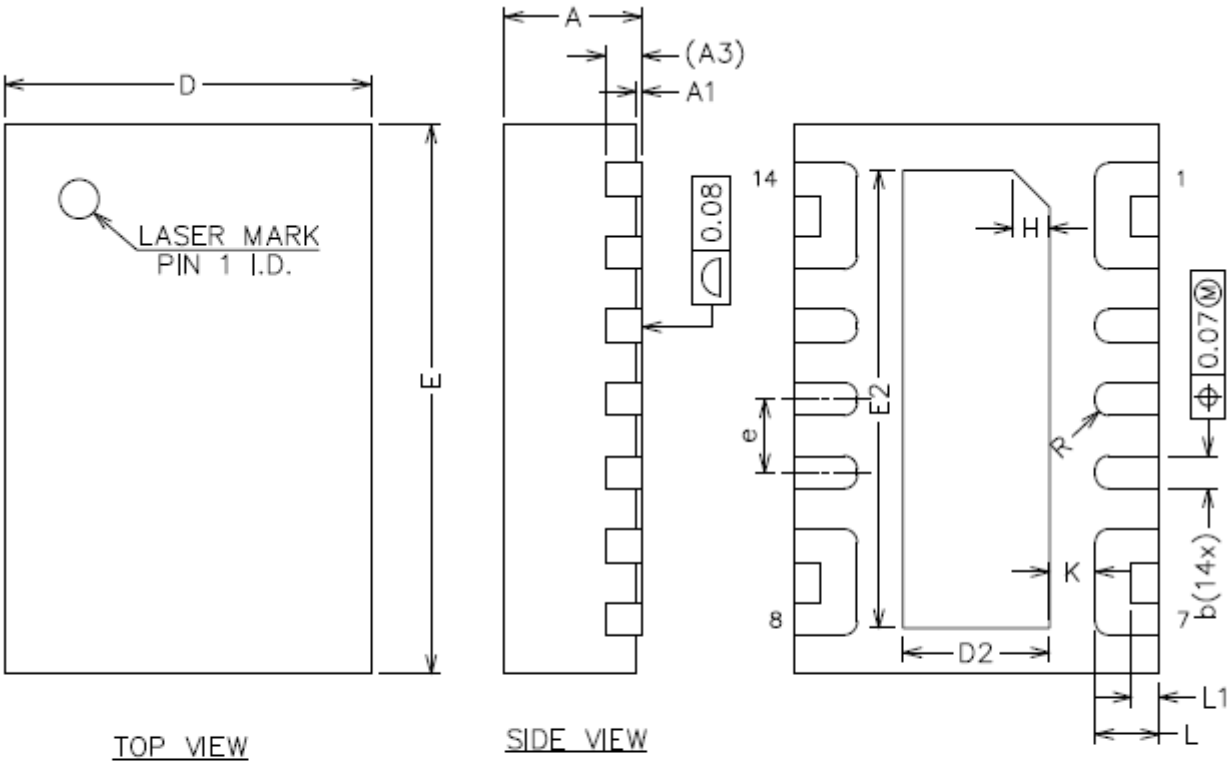
## Minimum Footprint PCB Layout Section

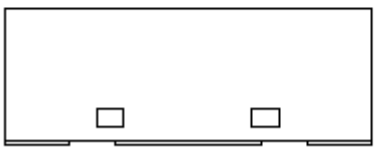
**TDFN2X3-14**



## Package Information

**TDFN2X3-14 Package**




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20REF | |
| b | 0.13 | 0.18 | 0.23 |
| D | 1.90 | 2.00 | 2.10 |
| E | 2.90 | 3.00 | 3.10 |
| D2 | 0.70 | 0.80 | 0.90 |
| E2 | 2.30 | 2.50 | 2.60 |
| e | 0.30 | 0.40 | 0.50 |
| H | | 0.20REF | |
| K | 0.15 | - | - |
| L | 0.30 | 0.35 | 0.40 |
| L1 | 0.10 | 0.15 | 0.20 |
| R | 0.05 | - | - |

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