

Description

The PSM8N10R9L uses split gate trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for power management and high efficiency applications at high switching frequencies applications.

MOSFET Product Summary

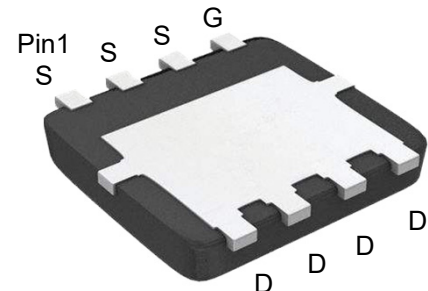
$V_{DS}(V)$	$R_{DS(on)}(m\Omega)(Typ)$	$I_D(A)$
100	7.0@ $V_{GS} = 10V$	70
	9.0@ $V_{GS} = 4.5V$	

Feature

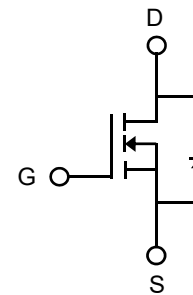
- Low $R_{DS(ON)}$ - Ensures On-State Losses are Minimized
- Excellent $Q_{gd} \times R_{DS(ON)}$ Product(FOM)
- Advanced Technology for DC-DC Converts
- Small Form Factor Thermally Efficient Package Enables Higher Density End Products
- 100% UIS (Avalanche) Rated
- Lead-Free Finish ; RoHS Compliant
- Halogen and Antimony Free. "Green" Device

Applications

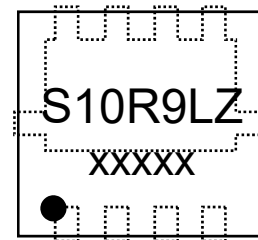
- PWM applications
- Load switch
- Power management
- DC-DC Converters
- Wireless Chargers



**PDFN5060-8L
(Bottom View)**



Circuit Diagram



**Pin1
Marking (Top View)**

Absolute maximum rating@25°C

Rating		Symbol	Value	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current-Continuous ¹⁾	$T_C=25^\circ C$	I_D	70	A
	$T_C=100^\circ C$		45	
Pulsed Drain Current ²⁾		I_{DM}	285	A
Total Power Dissipation ⁴⁾	$T_C=25^\circ C$	P_D	78	W
	$T_C=100^\circ C$		31	
Avalanche Current @ $L=0.1mH$		I_{AS}	32	A
Avalanche Energy @ $L=0.1mH$ ³⁾		E_{AS}	51	mJ
Thermal Resistance , Junction-to-Case ⁴⁾		$R_{\theta JC}$	1.6	$^\circ C/W$
Thermal Resistance Junction-to-Ambient ³⁾		$R_{\theta JA}$	45	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Off Characteristics							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$		100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V$	$T_J=25^{\circ}C$	-	-	1.0	μA
			$T_J=55^{\circ}C$	-	-	5.0	
Gate-Body Leakage Current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$		-	-	± 100	nA
On Characteristics ⁵⁾							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$		1.2	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 20A$		-	7.0	8.5	mΩ
		$V_{GS} = 4.5V, I_D = 15A$		-	9.0	10.8	
Forward Transconductance	g_{fs}	$V_{DS} = 5V, I_D = 20A$		-	30	-	S
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 2A$		-	0.7	1.2	V
Dynamic Characteristics ⁶⁾							
Input Capacitance	C_{Iss}	$V_{DS} = 50V, V_{GS} = 0V, f = 1.0MHz$		-	1295	-	pF
Output Capacitance	C_{oss}			-	615	-	
Reverse Transfer Capacitance	C_{rss}			-	14	-	
Gate Resistance	R_g	$V_{GS}=0V, V_{DS}=0V, f=1MHz$		-	1.5	-	Ω
Switching Characteristics ⁶⁾							
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 50V, V_{GS} = 10V, R_G = 3\Omega, I_D = 20A$		-	3.2	-	ns
Turn-on Rise Time	t_r			-	6.7	-	
Turn-Off Delay Time	$t_{d(off)}$			-	20	-	
Turn-Off Fall Time	t_f			-	14	-	
Total Gate Charge	Q_g	$V_{DS} = 560V, I_D = 20A, V_{GS}=0 \text{ to } 10V$		-	25	-	nC
Gate-Source Charge	Q_{gs}			-	3.6	-	
Gate-Drain Charge	Q_{gd}			-	5.4	-	
Drain-Source Diode Characteristics ⁶⁾							
Reverse Recovery Time	t_{rr}	$I_F=20A, d_I/d_t=100A/\mu s$		-	45	-	ns
Reverse Recovery Charge	Q_{rr}			-	53	-	nC
Diode Forward Current	I_S	-		-	-	70	A

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse test : Pulse width $\leq 100\mu s$, duty cycle $\leq 2\%$.
3. Device mounted on 1 inch FR4 PCB with 2oz.Copper.
4. Device mounted on infinite heatsink.
5. Measured under pulsed conditions. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
6. Guaranteed by design, not subject to production.

Typical Characteristics

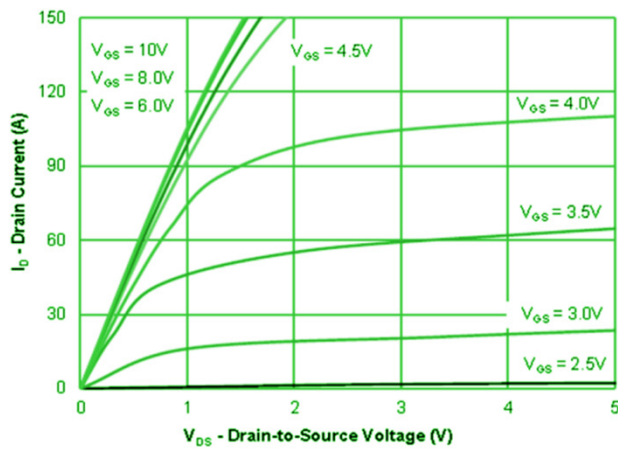


Figure 1: Output Characteristics

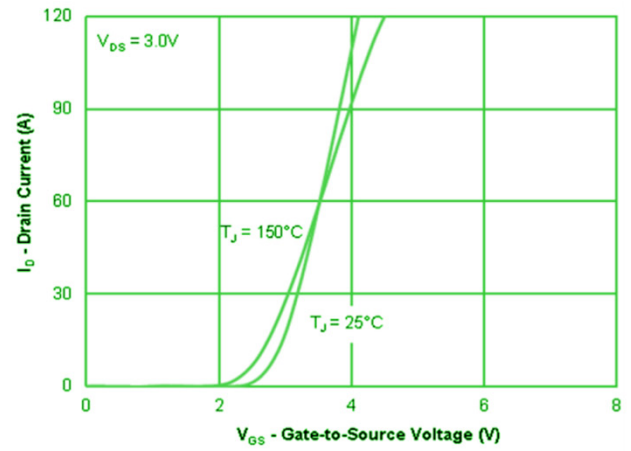


Figure 2: Transfer Characteristics

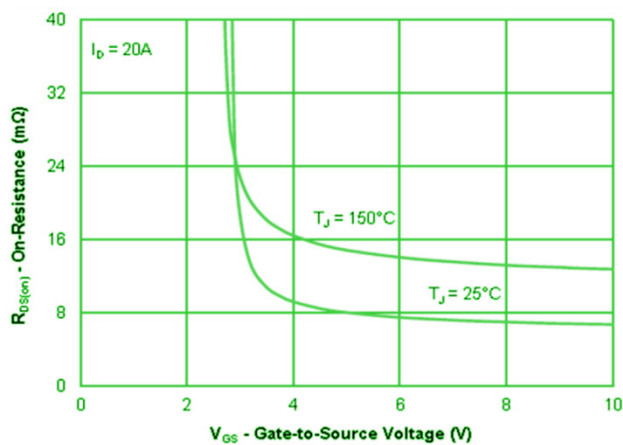


Figure 3: On-Resistance vs. Gate-Source Voltage

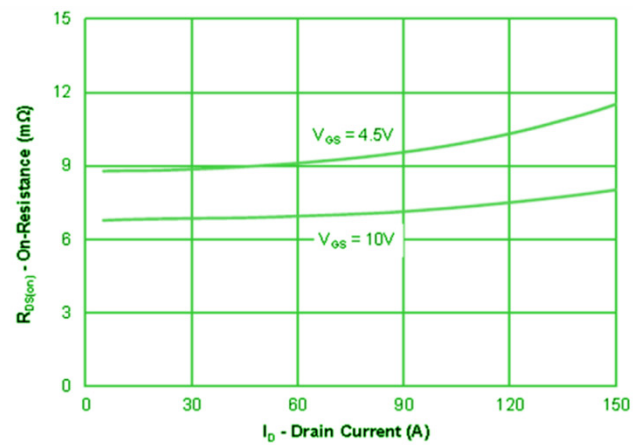


Figure 4: On-Resistance vs. Gate-Source Voltage

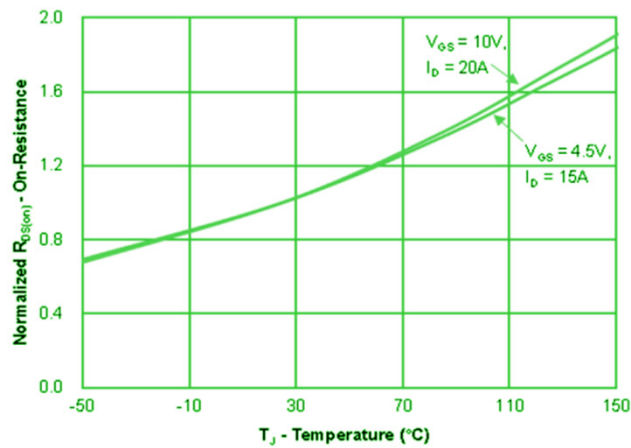


Figure 5: On-Resistance vs. Junction Temperature

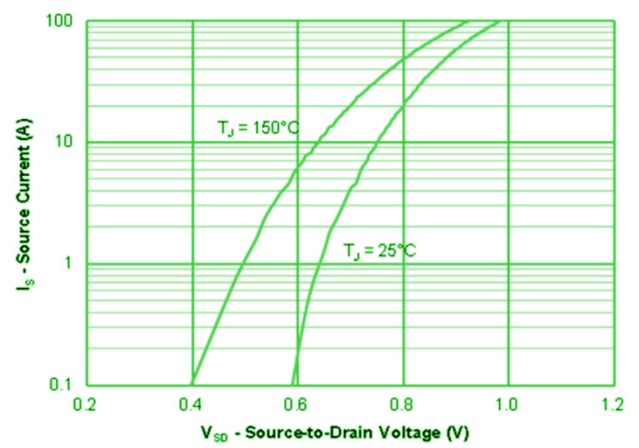


Figure 6: Source-Drain Diode Forward Voltage

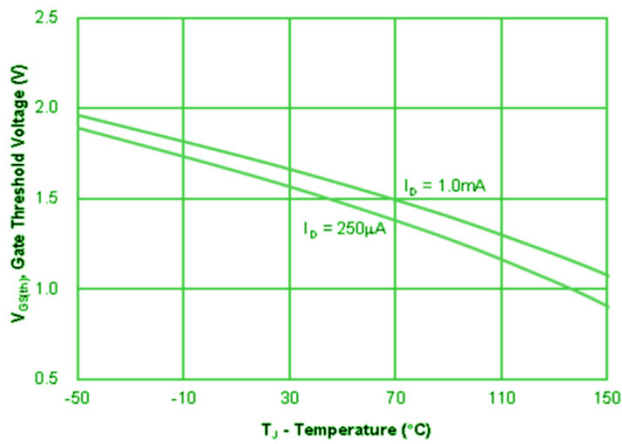


Figure 7: Gate Threshold Variation vs. Junction Temperature

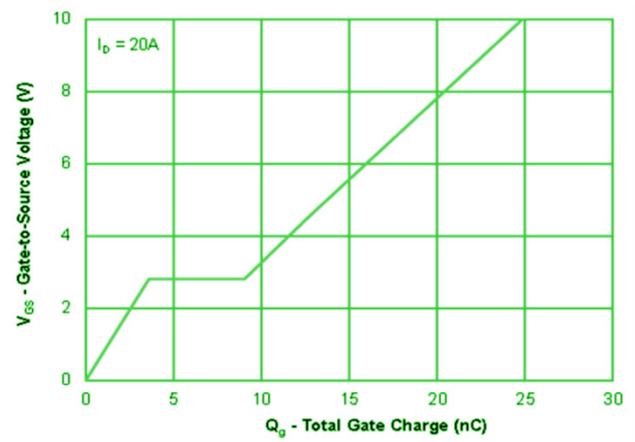


Figure 8: Gate Charge Characteristics

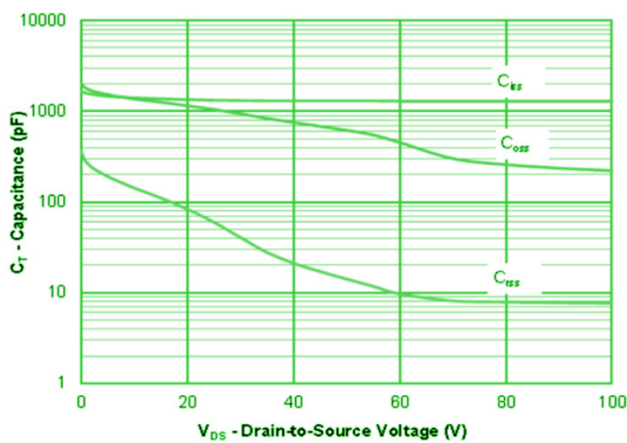


Figure 9: Capacitance Characteristics

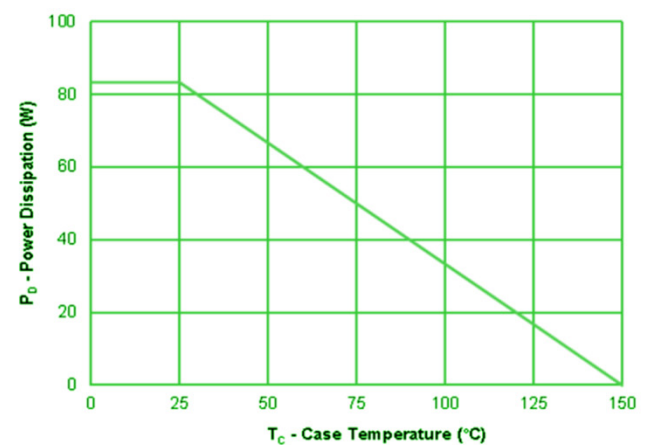


Figure 10: Power Derating

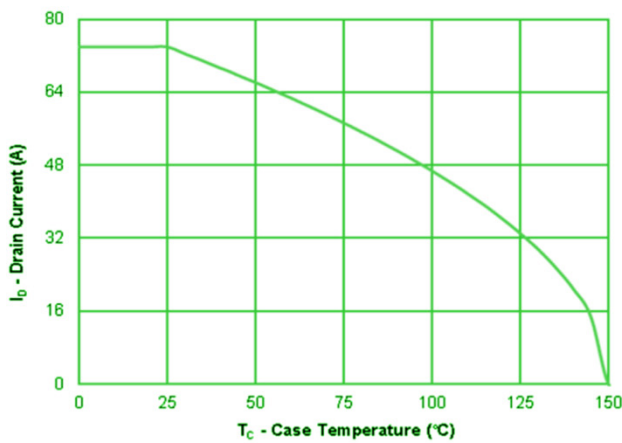


Figure 11: Current Derating

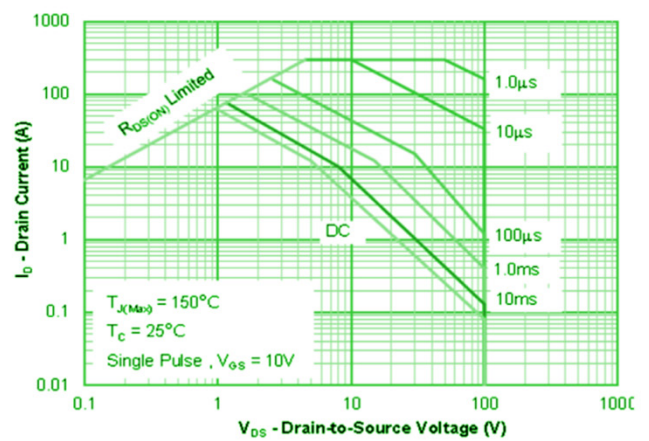


Figure 12: Safe Operating Area

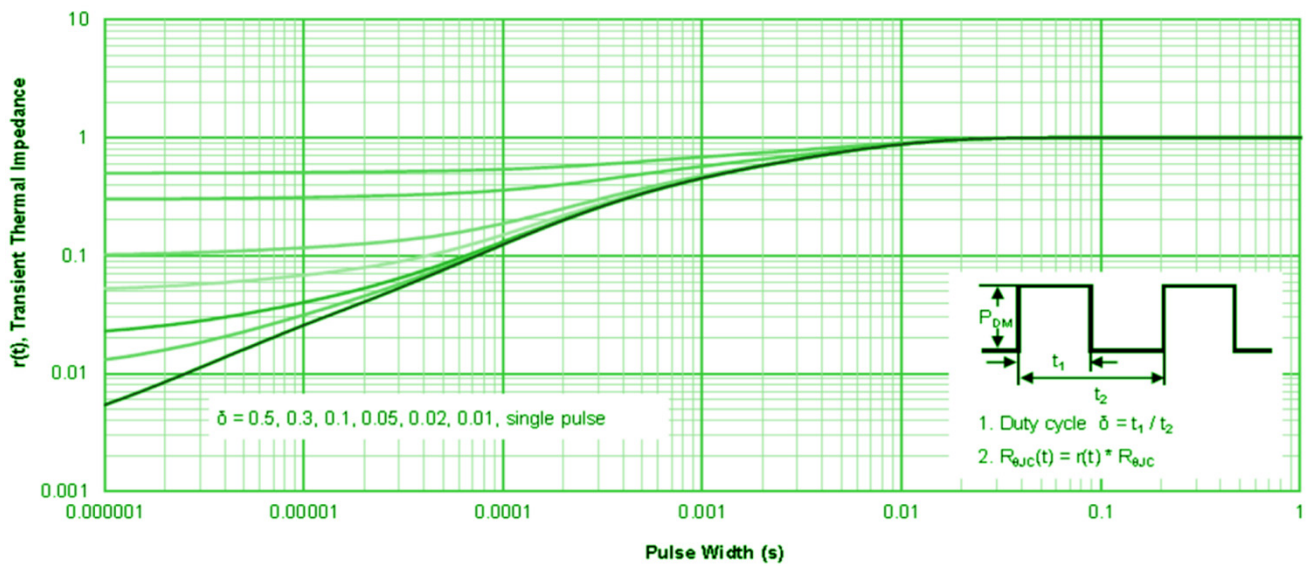
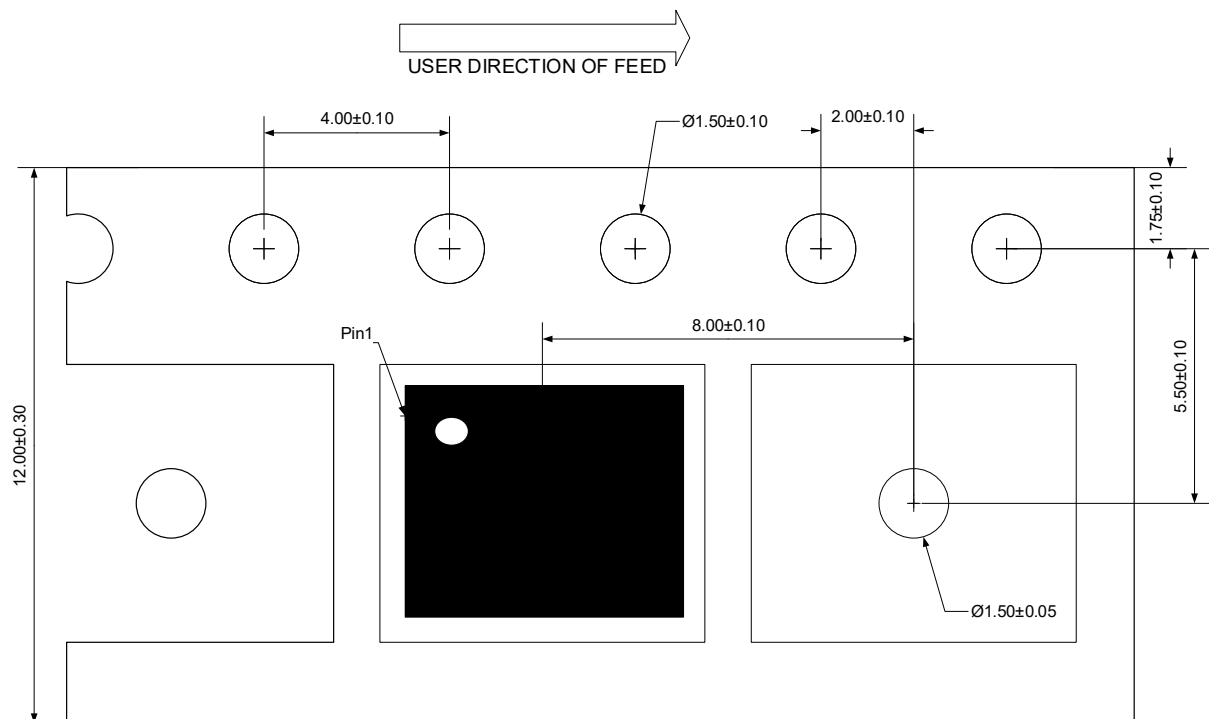


Figure 13: Normalized Maximum Transient Thermal Impedance

Ordering Information

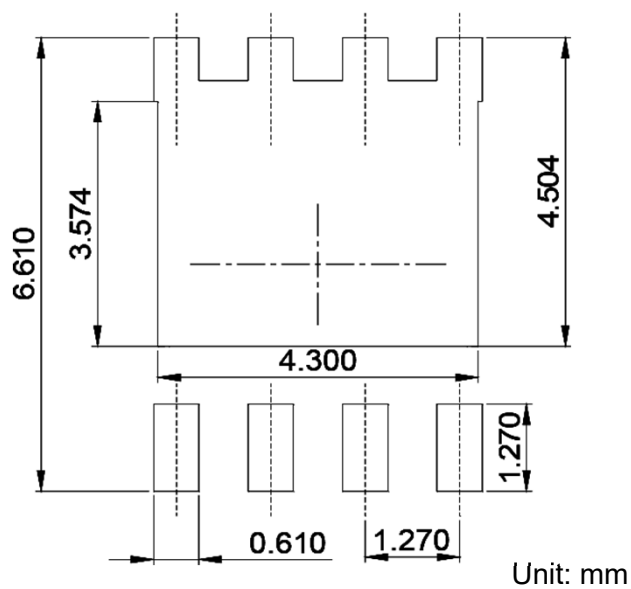
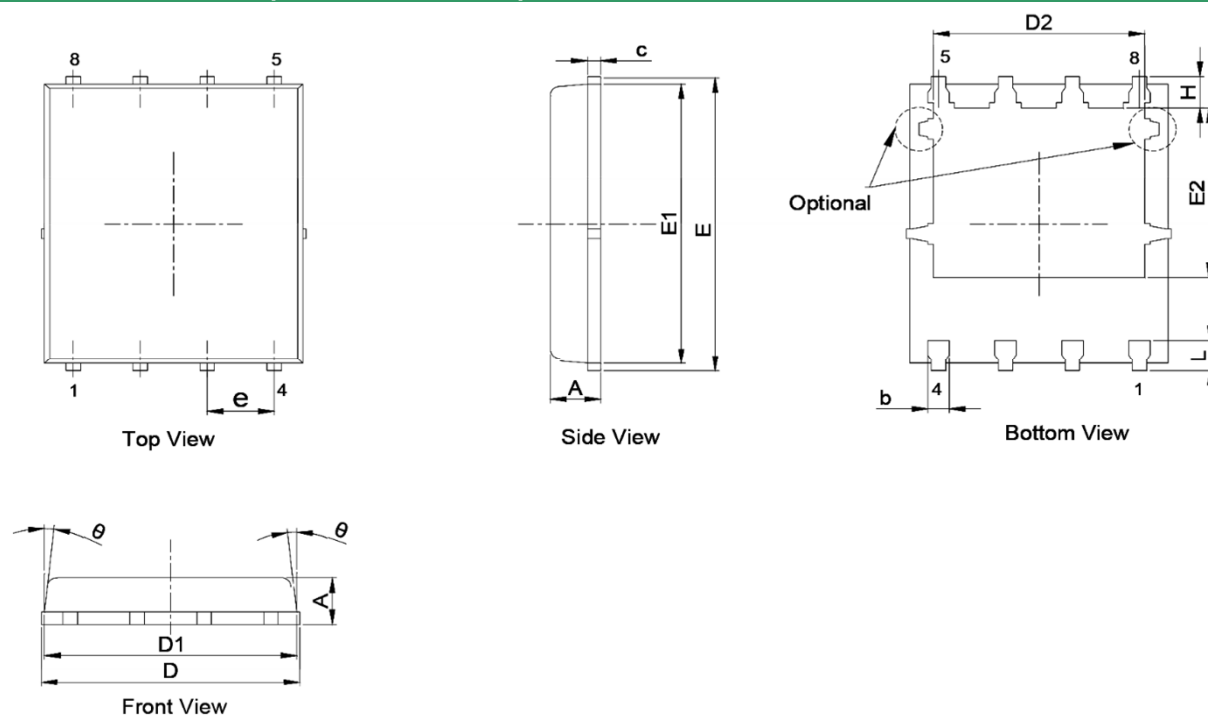
Package	Reel	Shipping
PDFN5060-8L	13"	5000 / Tape & Reel

Load With Information



Unit:mm

Product Dimension (PDFN5060-8L)



Suggested PCB Layout

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.10	0.035	0.043
b	0.25	0.51	0.010	0.020
c	0.15	0.30	0.006	0.012
D	5.00	5.40	0.197	0.213
D1	4.80	5.15	0.189	0.203
D2	3.90	4.20	0.154	0.165
E	5.90	6.25	0.232	0.246
E1	5.50	5.85	0.217	0.230
E2	3.35	3.63	0.132	0.143
e	1.27 BSC.		0.050 Ref.	
H	0.40	0.80	0.016	0.031
L	0.40	0.80	0.016	0.031
θ	-	12°	-	12°

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