

Description

The PSM8N04R5 uses split gate trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for power management and high efficiency applications at high switching frequencies applications.

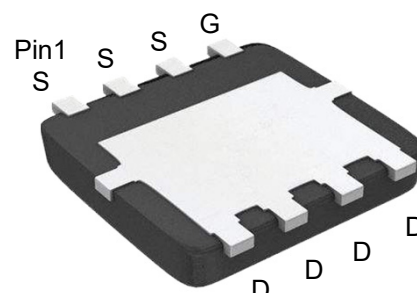
MOSFET Product Summary		
$V_{DS}(V)$	$R_{DS(on)}(m\Omega)$	$I_D(A)$
40	4.5@ $V_{GS} = 10V$	83
	7.2@ $V_{GS} = 4.5V$	

Feature

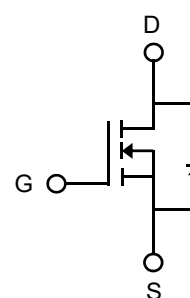
- Low $R_{DS(ON)}$ - Ensures On-State Losses are Minimized
- Excellent $Q_{gd} \times R_{DS(ON)}$ Product(FOM)
- Advanced Technology for DC-DC Converts
- Small Form Factor Thermally Efficient Package Enables Higher Density End Products
- 100% UIS (Avalanche) Rated
- Lead-Free Finish ; RoHS Compliant
- Halogen and Antimony Free. "Green" Device

Applications

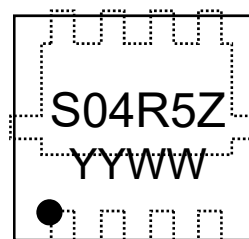
- PWM applications
- Load switch
- Power management
- DC-DC Converters
- Wireless Chargers



PDFN5060-8L
(Bottom View)



Circuit Diagram



Pin1
Marking (Top View)

Absolute maximum rating@25°C

Rating		Symbol	Value	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current-Continuous ¹⁾	$T_C=25^{\circ}C$	I_D	83	A
	$T_C=100^{\circ}C$		52	
Pulsed Drain Current ²⁾		I_{DM}	325	A
Total Power Dissipation ⁴⁾	$T_C=25^{\circ}C$	P_D	54	W
	$T_C=100^{\circ}C$		22	
Avalanche Current @ L=0.1mH		I_{AS}	25	A
Avalanche Energy @ L=0.1mH		E_{AS}	31	mJ
Thermal Resistance , Junction-to-Case ⁴⁾		$R_{\theta JC}$	2.3	$^{\circ}C/W$
Thermal Resistance Junction-to-Ambient ³⁾		$R_{\theta JA}$	48	$^{\circ}C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^{\circ}C$

Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Off Characteristics							
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA		40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V	T _J =25°C	-	-	1.0	μA
			T _J =55°C	-	-	5.0	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V		-	-	±100	nA
On Characteristics ⁵⁾							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA		1.2	1.7	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		-	3.7	4.5	mΩ
		V _{GS} = 4.5V, I _D = 15A		-	5.5	7.2	
Forward Transconductance	g _{fs}	V _{DS} = 5 V, I _D = 20A		-	25	-	S
Diode Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = 2A		-	0.7	1.2	V
Dynamic Characteristics ⁶⁾							
Input Capacitance	C _{iss}	V _{DS} = 20V, V _{GS} = 0V, f = 1.0MHz		-	1000	-	pF
Output Capacitance	C _{oss}			-	600	-	
Reverse Transfer Capacitance	C _{rss}			-	25	-	
Switching Characteristics ⁶⁾							
Turn-on Delay Time	t _{d(on)}	V _{DS} = 20V, V _{GS} = 10V, R _G = 3Ω, I _D = 20A		-	2.0	-	ns
Turn-on Rise Time	t _r			-	15	-	
Turn-Off Delay Time	t _{d(off)}			-	20	-	
Turn-Off Fall Time	t _f			-	15	-	
Total Gate Charge	Q _g	V _{DS} = 20V, I _D = 20A, V _{GS} = 0 to 10V,		-	15	-	nC
Gate-Source Charge	Q _{gs}			-	7.0	-	
Gate-Drain Charge	Q _{gd}			-	3.5	-	
Gate Resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz		-	2.0	-	Ω
Drain-Source Diode Characteristics ⁶⁾							
Body Diode Reverse Recovery Time	t _{rr}	I _F =20A, d _I /d _t =100A/μs		-	35	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	15	-	nC
Diode Forward Current	I _S	-		-	-	82	A

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse test : Pulse width $\leq 100\mu s$, duty cycle $\leq 2\%$.
3. Device mounted on 1 inch FR4 PCB with 2oz.Copper.
4. Device mounted on infinite heatsink.
5. Measured under pulsed conditions. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
6. Guaranteed by design, not subject to production.

Typical Characteristics

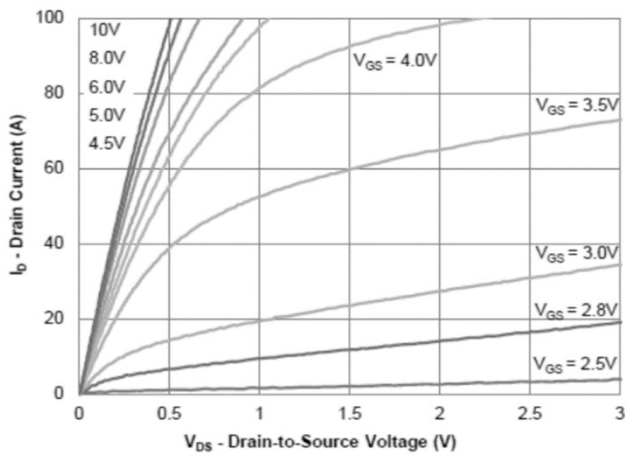


Figure 1: Output Characteristics

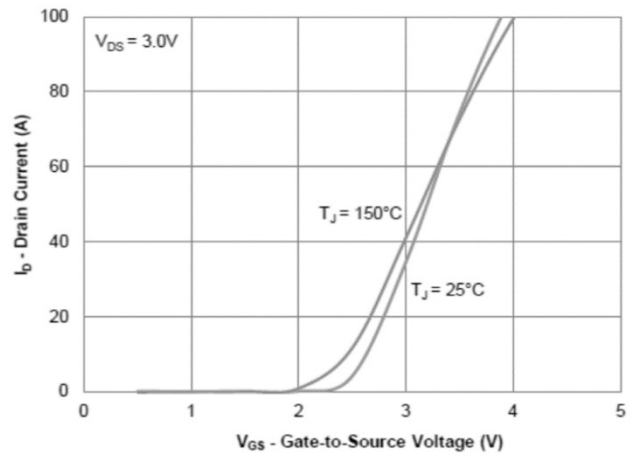


Figure 2: Transfer Characteristics

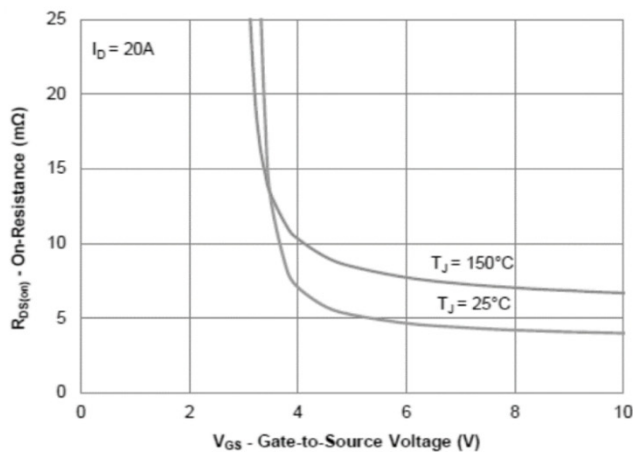


Figure 3: On-Resistance vs. Gate-Source Voltage

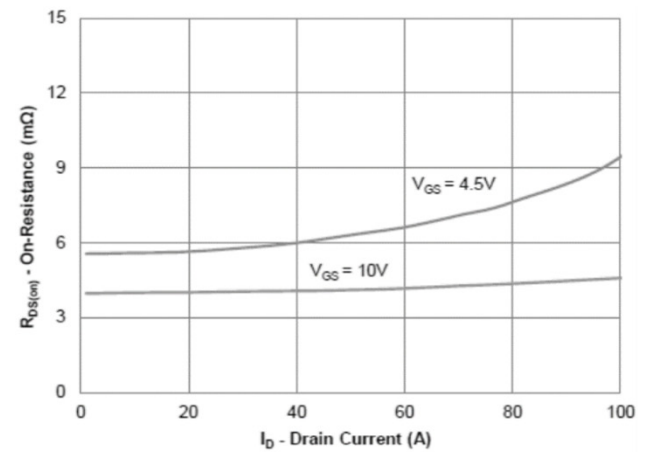


Figure 4: On-Resistance vs. Gate-Source Voltage

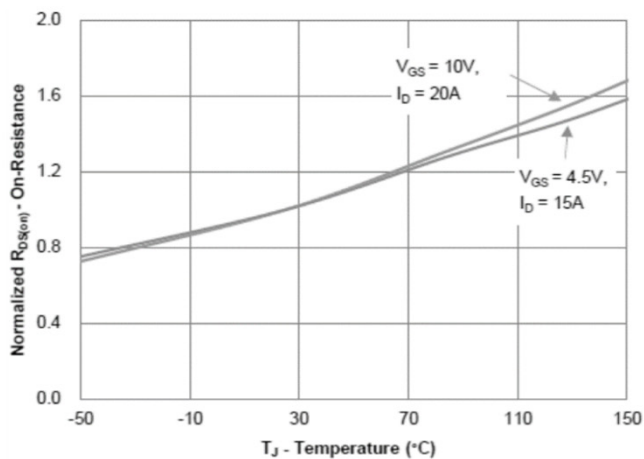


Figure 5: On-Resistance vs. Junction Temperature

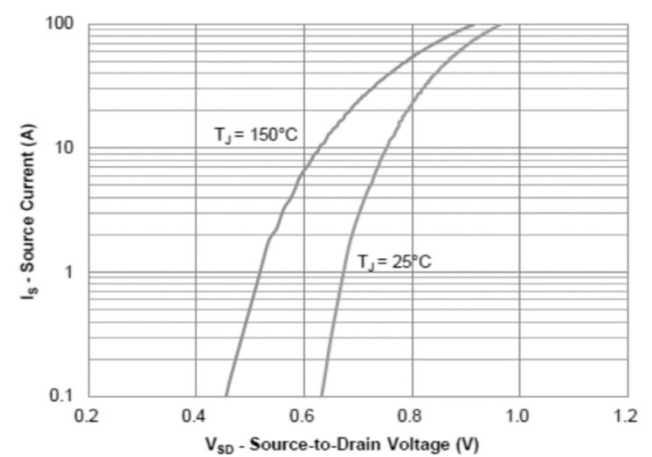


Figure 6: Source-Drain Diode Forward Voltage

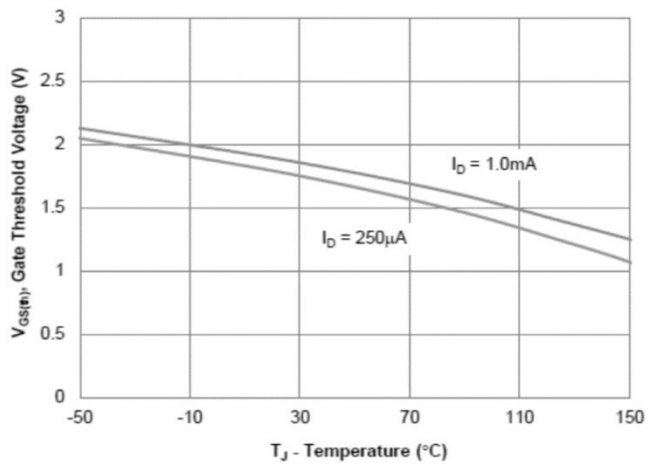


Figure 7: Gate Threshold Variation vs. Junction Temperature

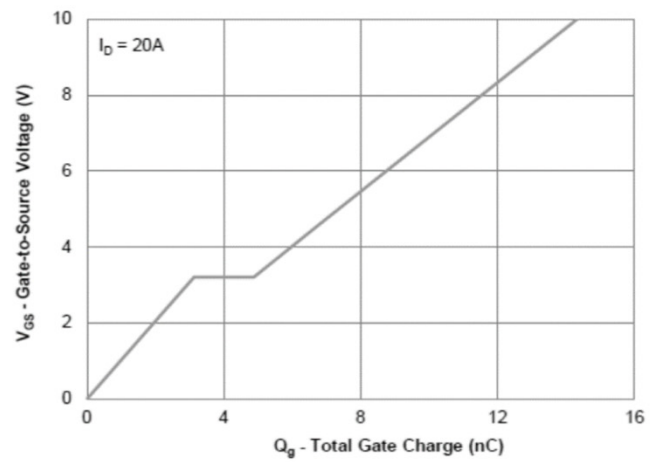


Figure 8: Gate Charge Characteristics

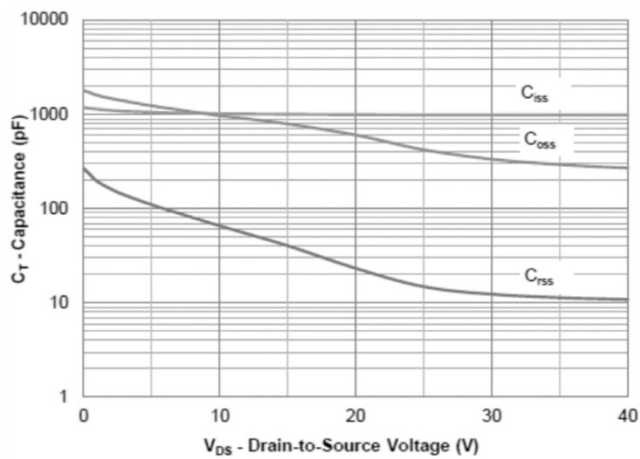


Figure 9: Capacitance Characteristics

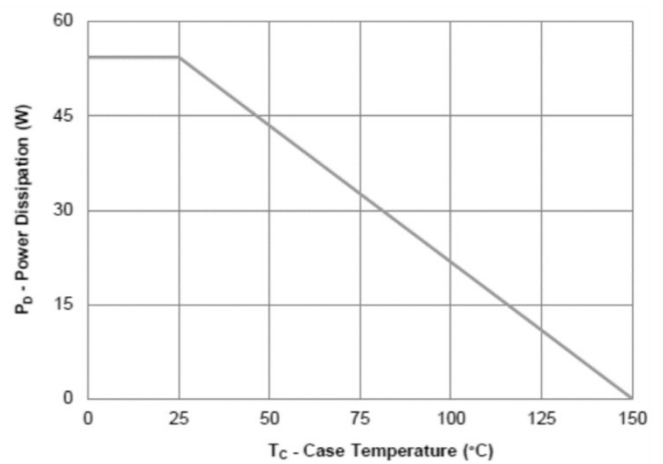


Figure 10: Power Derating

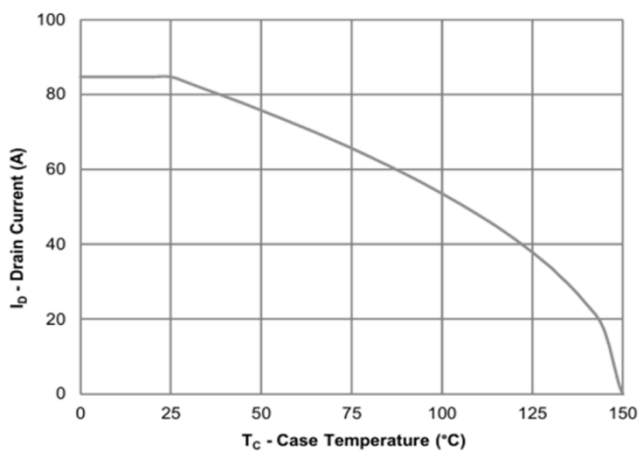


Figure 11: Current Derating

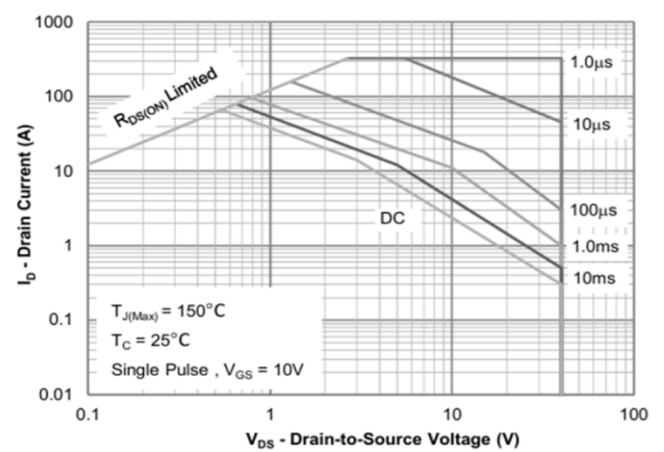


Figure 12: Safe Operating Area

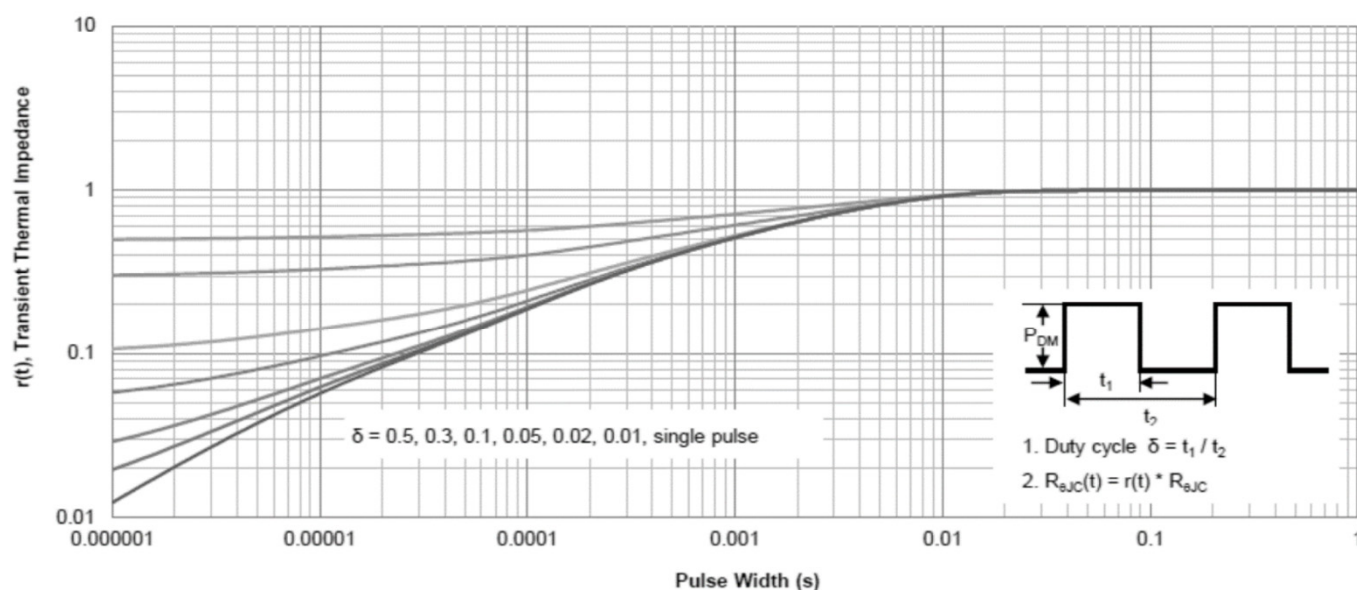
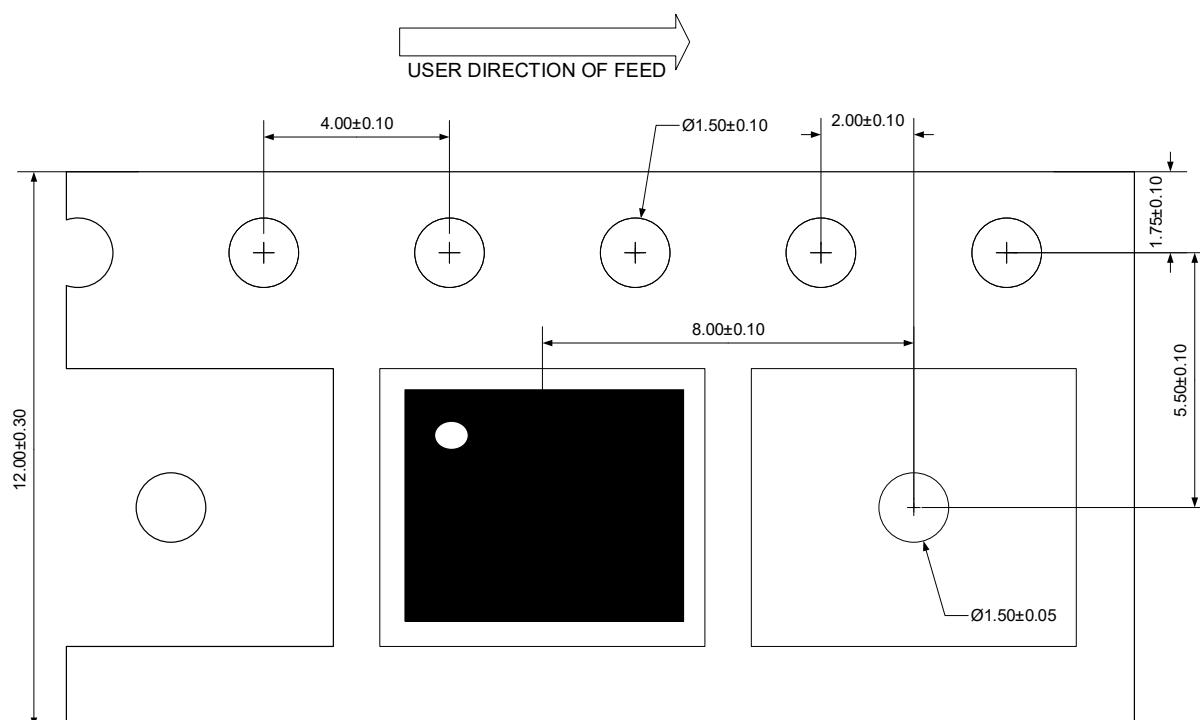


Figure 13: Normalized Maximum Transient Thermal Impedance

Ordering Information

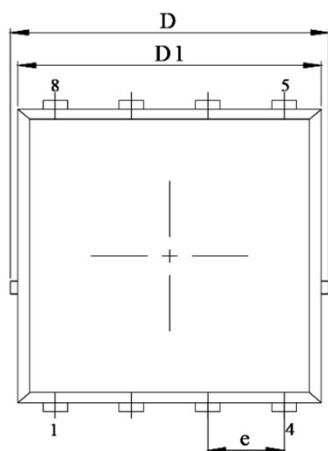
Device	Package	Reel	Shipping
PSM8N04R5	PDFN5060-8L	13"	5000 / Tape & Reel

Load With Information

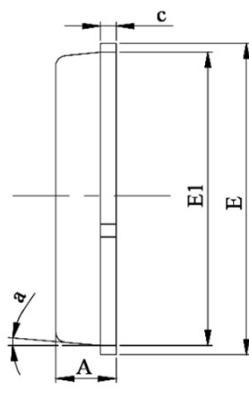


Unit:mm

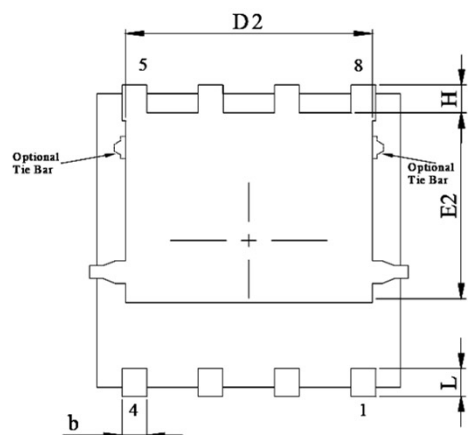
Product Dimension (PDFN5060-8L)



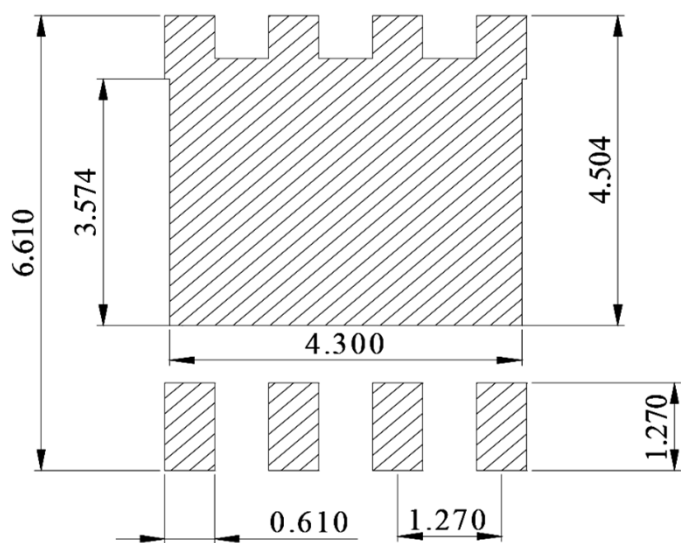
Top View



Side View



Bottom View



Unit: mm

Suggested PCB Layout

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.10	0.035	0.043
b	0.25	0.51	0.010	0.020
c	0.15	0.30	0.006	0.012
D	5.00	5.40	0.197	0.213
D1	4.80	5.15	0.189	0.203
D2	3.90	4.20	0.154	0.165
E	5.90	6.10	0.232	0.240
E1	5.50	5.85	0.217	0.230
E2	3.35	3.63	0.132	0.143
e	1.27 BSC.		0.050 BSC.	
H	0.40	0.80	0.016	0.031
L	0.40	0.80	0.016	0.031
a	-	12°	-	12°

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