

Description

The PSM8N04R08L uses split gate trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for power management and high efficiency applications at high switching frequencies applications.

MOSFET Product Summary

$V_{DS}(V)$	$R_{DS(on)}(m\Omega)(Typ)$	$I_D(A)$
40	0.7@ $V_{GS} = 10V$	320
	0.95@ $V_{GS} = 4.5V$	

Feature

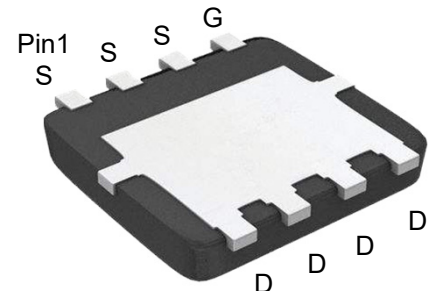
- Excellent $R_{DS(ON)}$
- Low Gate Charge
- Fast Switching Speed

Applications

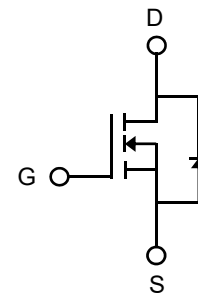
- Motor drives
- Load switching
- Hard Switching and High Speed Circuit

Mechanical Data

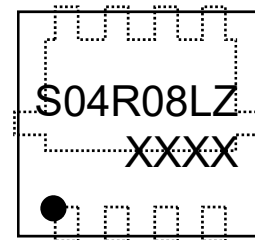
- Case: PDFN5060-8L
- Moisture Sensitivity: Level 1 per J-STD-020
- Case Material: "Green" Molding Compound.
UL Flammability Classification Rating 94V-0



**PDFN5060-8L
(Bottom View)**



Circuit Diagram



**Pin1
Marking (Top View)**

Absolute maximum rating@25°C

Rating		Symbol	Value	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current-Continuous ¹⁾	$T_C=25^\circ C$	I_D	320	A
	$T_C=100^\circ C$		200	
Pulsed Drain Current ²⁾		I_{DM}	1285	A
Total Power Dissipation ⁴⁾	$T_C=25^\circ C$	P_D	130	W
	$T_C=100^\circ C$		51	
Avalanche Current @ $L=0.3mH$		I_{AS}	50	A
Avalanche Energy @ $L=0.3mH$		E_{AS}	375	mJ
Thermal Resistance , Junction-to-Case ⁴⁾		$R_{\theta JC}$	0.9	$^\circ C/W$
Thermal Resistance Junction-to-Ambient ³⁾		$R_{\theta JA}$	35	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Off Characteristics							
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA		40	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40V, V _{GS} = 0V	T _J =25°C	-	-	1.0	μA
			T _J =55°C	-	-	5.0	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V		-	-	±100	nA
On Characteristics ⁵⁾							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA		1.2	1.7	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A		-	0.7	0.85	mΩ
		V _{GS} = 4.5V, I _D = 15A		-	0.95	1.25	
Forward Transconductance	g _{fs}	V _{DS} = 5 V, I _D = 20A		-	85	-	S
Diode Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = 2A		-	0.7	1.2	V
Dynamic Characteristics ⁶⁾							
Input Capacitance	C _{iss}	V _{DS} = 20V, V _{GS} = 0V, f = 1.0MHz		-	5589	-	pF
Output Capacitance	C _{oss}			-	3315	-	
Reverse Transfer Capacitance	C _{rss}			-	121	-	
Gate Resistance	R _g	V _{GS} =0V, V _{DS} =0V, f=1MHz		-	2.5	-	Ω
Switching Characteristics ⁶⁾							
Turn-on Delay Time	t _{d(on)}	V _{DS} = 20V, V _{GS} = 10V, R _G = 3Ω, I _D = 20A		-	5.3	-	ns
Turn-on Rise Time	t _r			-	12	-	
Turn-Off Delay Time	t _{d(off)}			-	68	-	
Turn-Off Fall Time	t _f			-	37	-	
Total Gate Charge @ V _{GS} = 10V	Q _g	V _{DS} = 20V, I _D = 20A, V _{GS} = 10V		-	85	-	nC
Gate-Source Charge	Q _{gs}			-	15	-	
Gate-Drain Charge	Q _{gd}			-	13	-	
Drain-Source Diode Characteristics ⁶⁾							
Reverse Recovery Time	t _{rr}	I _F =20A, d _I /d _t =100A/μs		-	65	-	ns
Reverse Recovery Charge	Q _{rr}			-	123	-	nC
Diode Forward Current	I _S	-		-	-	130	A

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse test : Pulse width $\leq 100\mu s$, duty cycle $\leq 2\%$.
3. Device mounted on 1 inch FR4 PCB with 2oz.Copper.
4. Device mounted on infinite heatsink.
5. Measured under pulsed conditions. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
6. Guaranteed by design, not subject to production.

Typical Characteristics

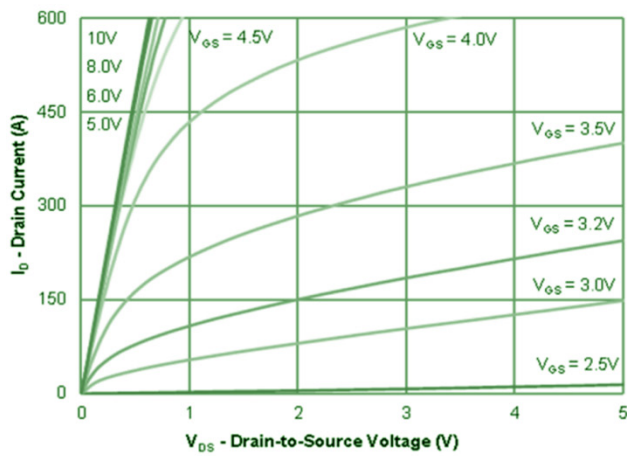


Figure 1: Output Characteristics

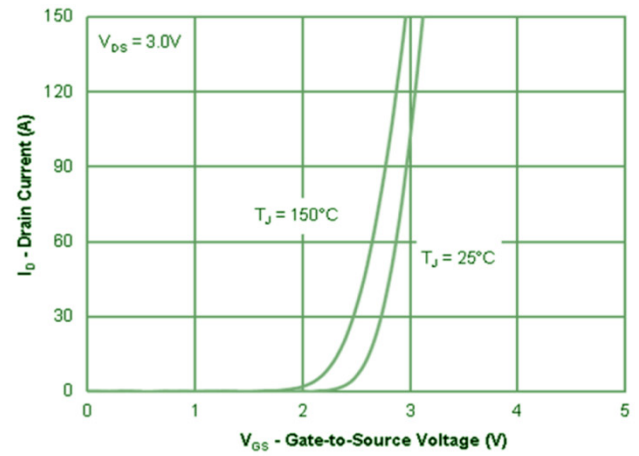


Figure 2: Transfer Characteristics

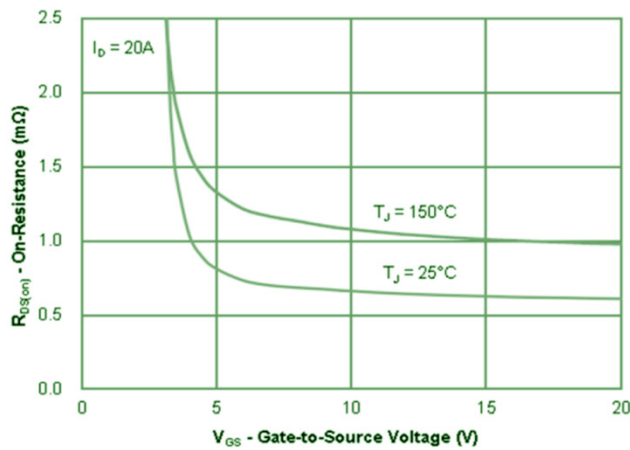


Figure 3: On-Resistance vs. Gate-Source Voltage

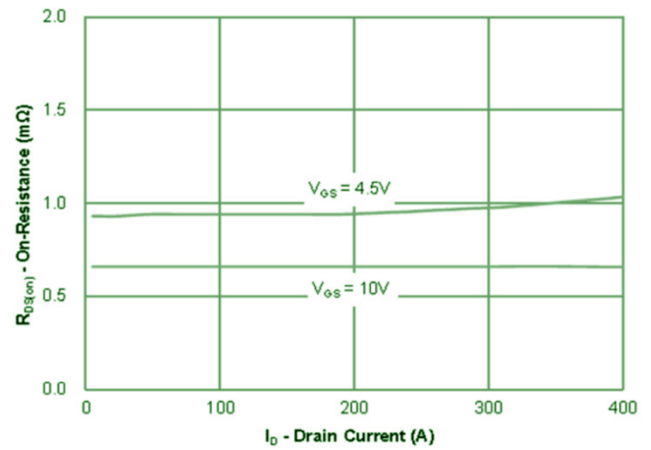


Figure 4: On-Resistance vs. Gate-Source Voltage

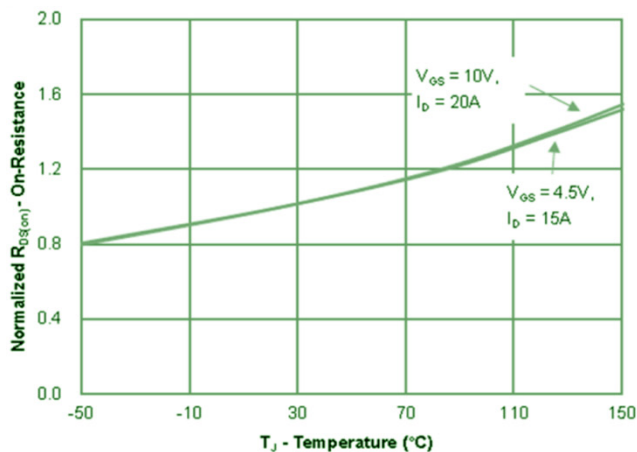


Figure 5: On-Resistance vs. Junction Temperature

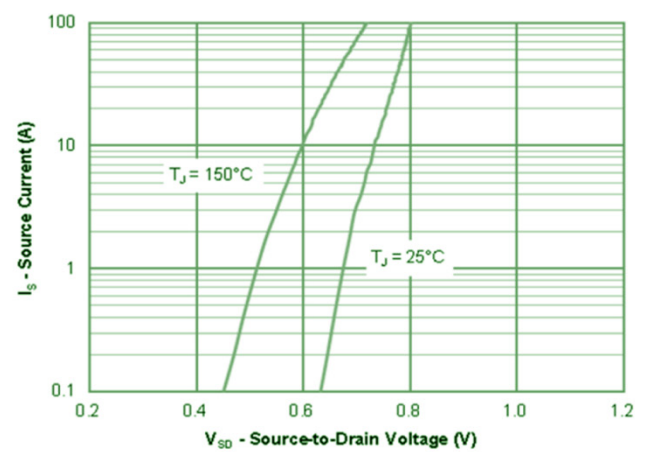


Figure 6: Source-Drain Diode Forward Voltage

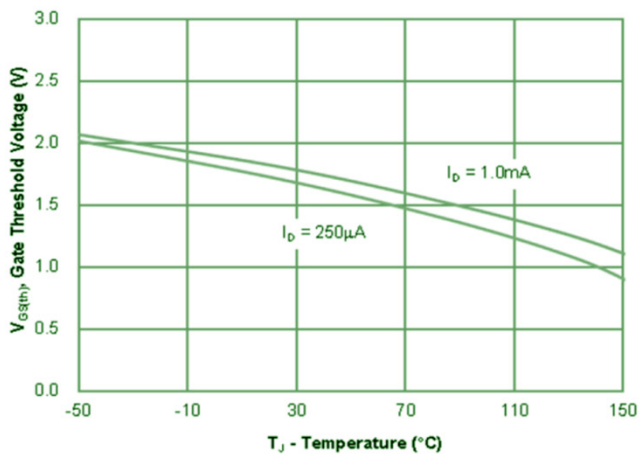


Figure 7: Gate Threshold Variation vs. Junction Temperature

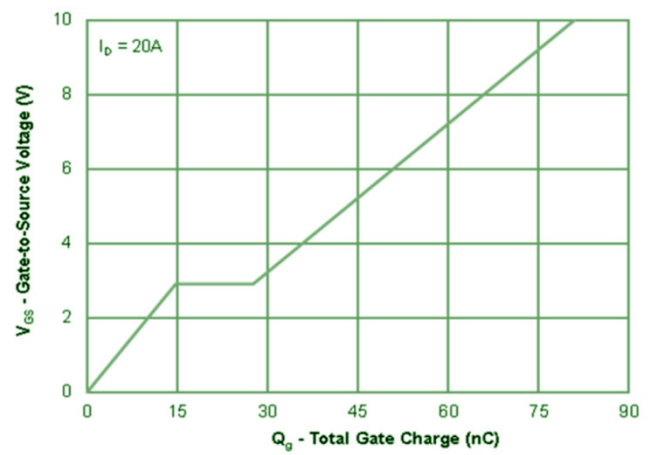


Figure 8: Gate Charge Characteristics

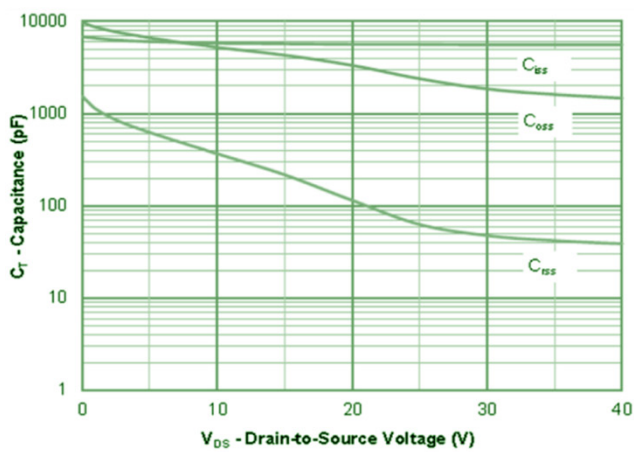


Figure 9: Capacitance Characteristics

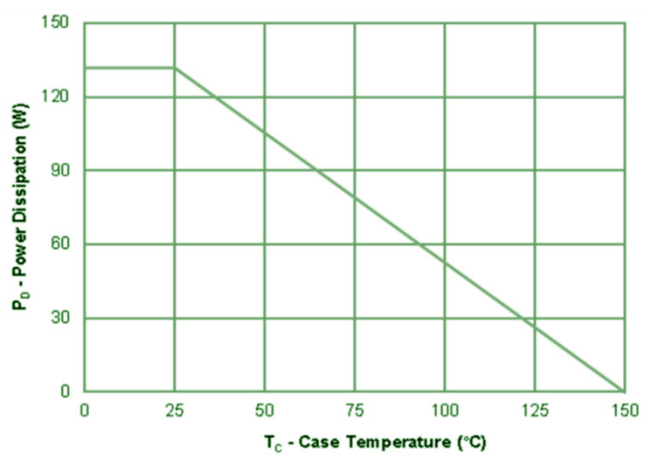


Figure 10: Power Derating

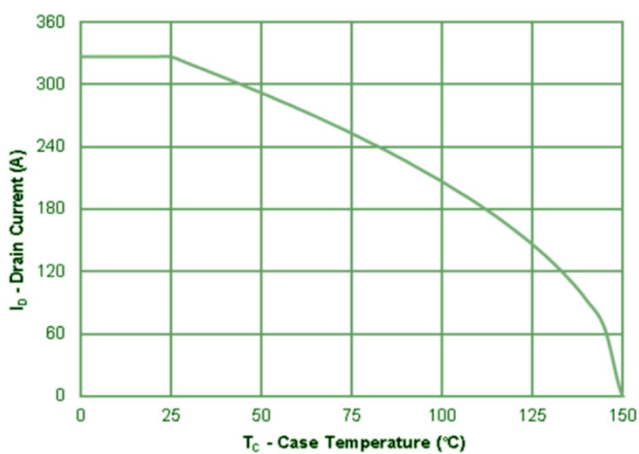


Figure 11: Current Derating

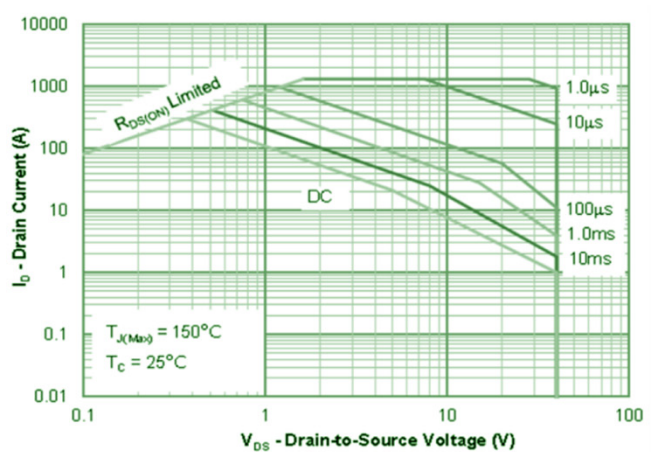


Figure 12: Safe Operating Area

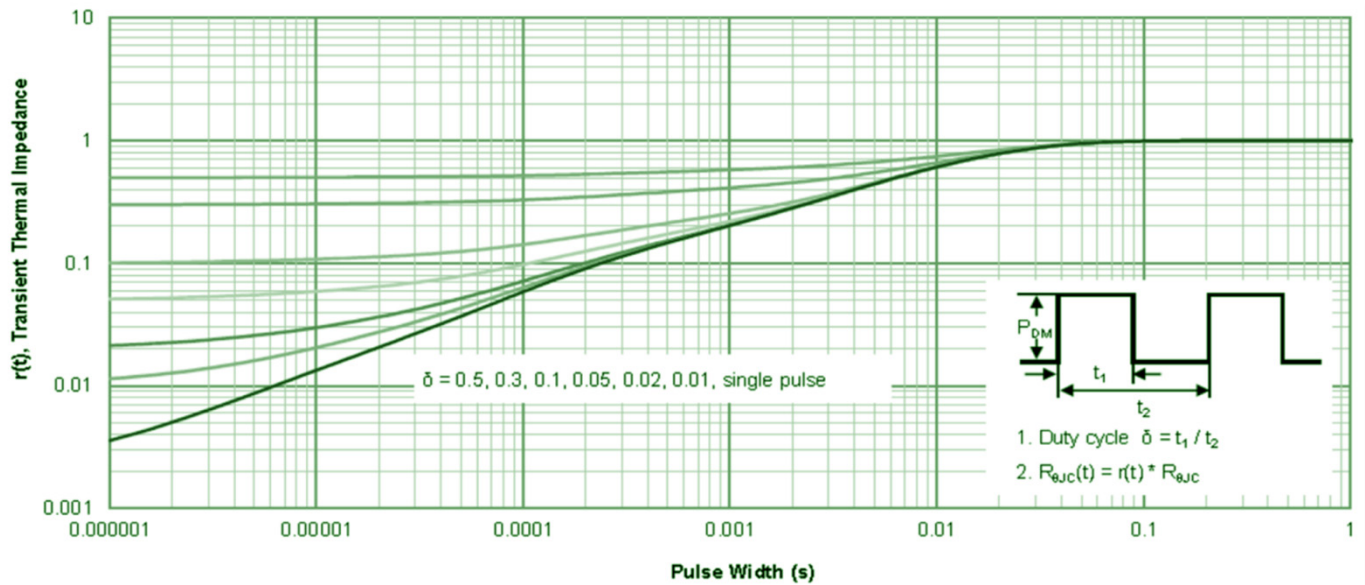
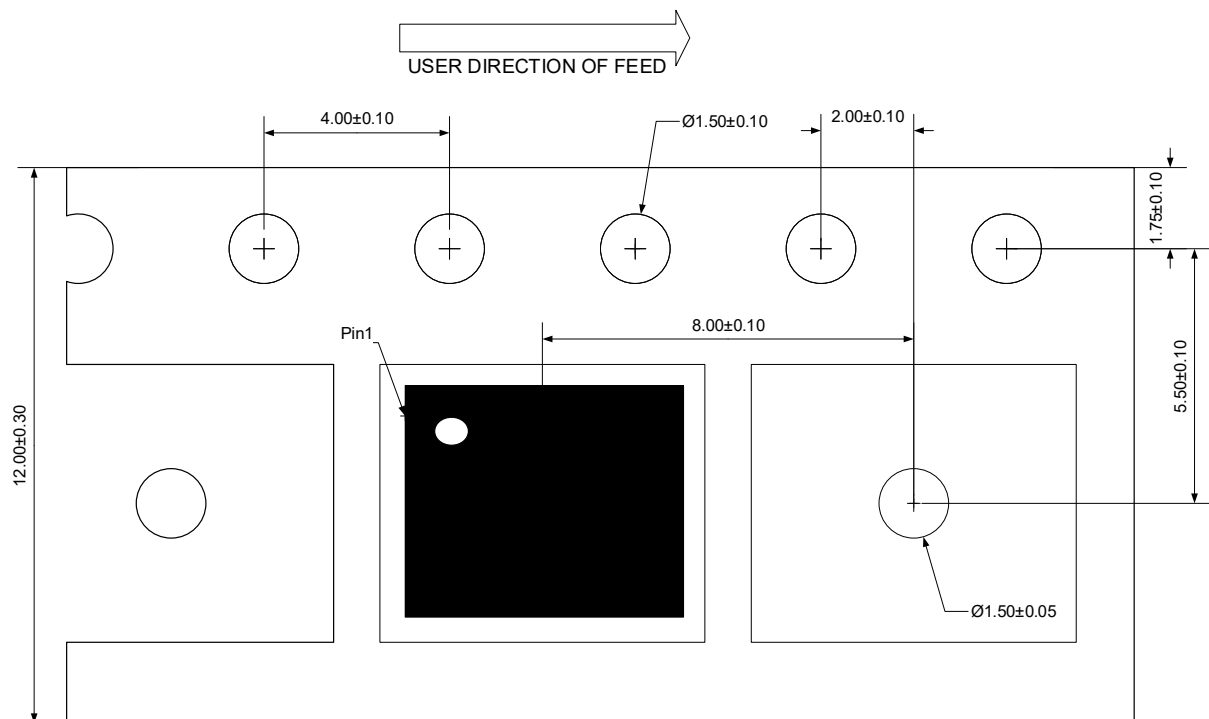


Figure 13: Normalized Maximum Transient Thermal Impedance

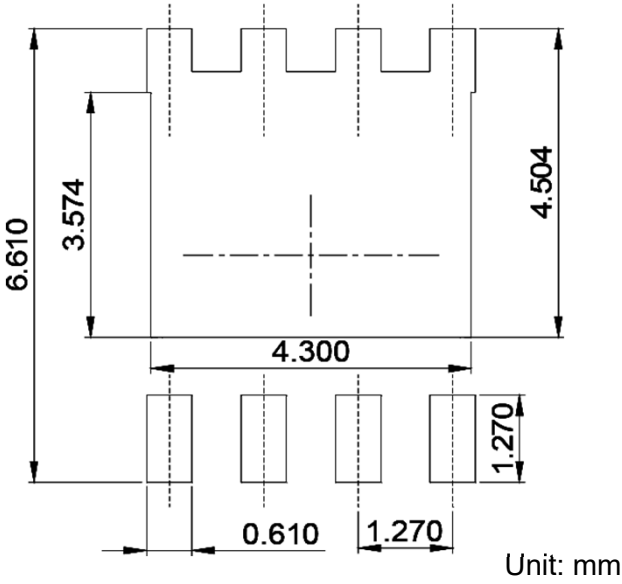
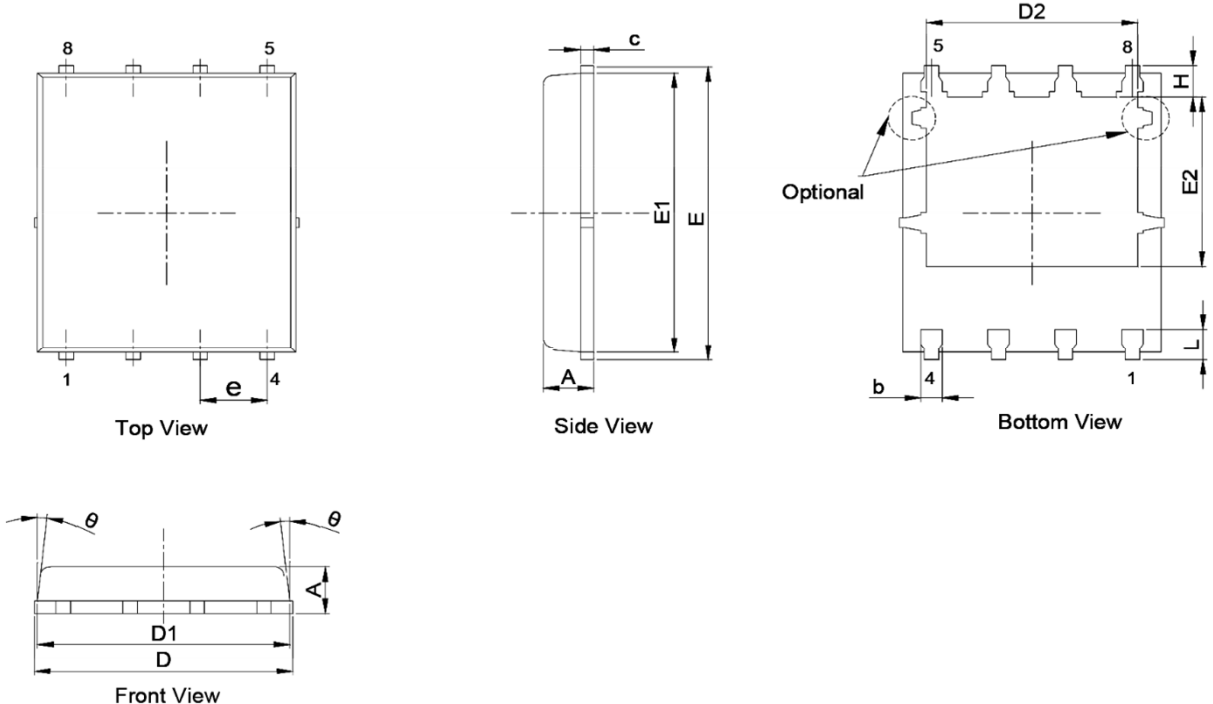
Ordering Information

Package	Reel	Shipping
PDFN5060-8L	13"	5000 / Tape & Reel

Load With Information



Product Dimension (PDFN5060-8L)



Suggested PCB Layout

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.20	0.035	0.047
b	0.30	0.51	0.012	0.020
c	0.20	0.34	0.008	0.013
D	4.80	5.40	0.189	0.213
D1	4.65	5.30	0.183	0.209
D2	3.60	4.25	0.142	0.167
E	5.90	6.50	0.232	0.256
E1	5.70	6.00	0.224	0.236
E2	3.38	3.92	0.133	0.154
e	1.27 BSC.		0.050 Ref.	
H	0.40	0.93	0.016	0.037
L	0.40	0.91	0.016	0.036
θ	0°	12°	0°	12°

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