

Description

The PDSM8N03R5L uses split gate trench technology to provide excellent $R_{DS(on)}$ and low gate charge. This device is suitable for power management and high efficiency applications at high switching frequencies applications.

MOSFET Product Summary

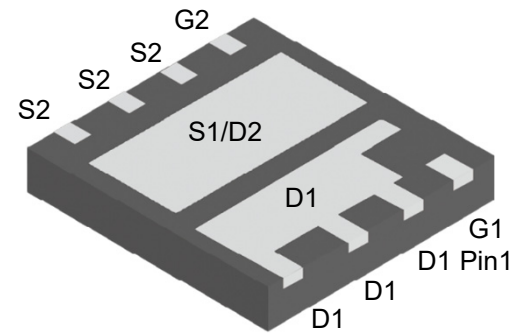
$V_{DS}(V)$	$R_{DS(on)}(m\Omega)(Typ)$	$I_D(A)$
30	4.1@ $V_{GS} = 10V$	70
	5.6@ $V_{GS} = 4.5V$	

Feature

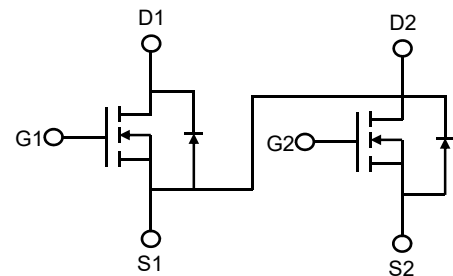
- Low $R_{DS(on)}$ - Ensures On-State Losses are Minimized
- Excellent $Q_{gd} \times R_{DS(on)}$ Product(FOM)
- Advanced Technology for DC-DC Converts
- Small Form Factor Thermally Efficient Package
Enables Higher Density End Products
- 100% UIS (Avalanche) Rated
- Lead-Free Finish ; RoHS Compliant
- Halogen and Antimony Free. "Green" Device

Applications

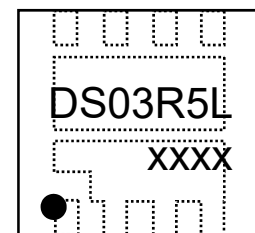
- PWM applications
- Load switch
- Power management
- DC-DC Converters
- Wireless Chargers



**DFN5060-8L
(Bottom View)**



Circuit Diagram



Pin1

Marking (Top View)

Absolute maximum rating@25°C

Rating		Symbol	Value	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current-Continuous ¹⁾	$T_C = 25^\circ C$	I_D	70	A
	$T_C = 100^\circ C$		44.5	
Pulsed Drain Current ²⁾		I_{DM}	280	A
Total Power Dissipation ³⁾		P_D	40	W
Avalanche Current ⁴⁾		I_{AS}	30	A
Avalanche Energy ⁴⁾		E_{AS}	45	mJ
Thermal Resistance Junction-to-Case ⁵⁾		$R_{\theta JC}$	3.1	$^\circ C/W$
Thermal Resistance Junction-to-Ambient ⁶⁾		$R_{\theta JA}$	54.5	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ C$

Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30V, V _{GS} = 0V	-	-	1.0	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A	-	4.1	5.2	mΩ
		V _{GS} = 4.5V, I _D = 15A	-	5.6	7.0	
Dynamic Characteristics ⁷⁾						
Input Capacitance	C _{iss}	V _{DS} = 15V, V _{GS} = 0V, f = 1MHz	-	927	-	pF
Output Capacitance	C _{oss}		-	272	-	
Reverse Transfer Capacitance	C _{rss}		-	28	-	
Switching Characteristics ⁷⁾						
Turn-on Delay Time	t _{d(on)}	V _{DS} = 15V, V _{GS} = 10V, I _D = 20A, R _G = 10Ω	-	4.3	-	ns
Turn-on Rise Time	t _r		-	5.3	-	
Turn-Off Delay Time	t _{d(off)}		-	26.1	-	
Turn-Off Fall Time	t _f		-	14.6	-	
Total Gate Charge	Q _g	V _{DS} = 15V, V _{GS} = 10V, I _D = 20A	-	14.2	-	nC
Gate-Source Charge	Q _{gs}		-	2.1	-	
Gate-Drain Charge	Q _{gd}		-	4.3	-	
Gate Resistance	R _g	f=1MHz, Open Drain	-	4.1	-	Ω
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = 15A	0.5	0.9	1.2	V
Reverse Recovery Time	t _{rr}	I _F =15A, di/dt=100A/us	-	15.5	-	ns
Reverse Recovery Charge	Q _{rr}		-	5.4	-	nC

Notes:

1. Computed continuous current assumes the condition of T_{J_Max} while the actual continuous current depends on the thermal & electro-mechanical application board design.
2. Repetitive Rating: Pulse width limited by maximum junction temperature($T_{J_Max}=150^\circ C$).
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. This single-pulse measurement was taken under the following condition [$L=0.1mH, V_{GS}=10V, V_{DS}=30V$]while it's value is limited by $T_{J_Max}=150^\circ C$.
5. Device mounted on infinite heatsink.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1 inch square copper pad layout.
7. Guaranteed by design, not subject to production.

Typical Characteristics

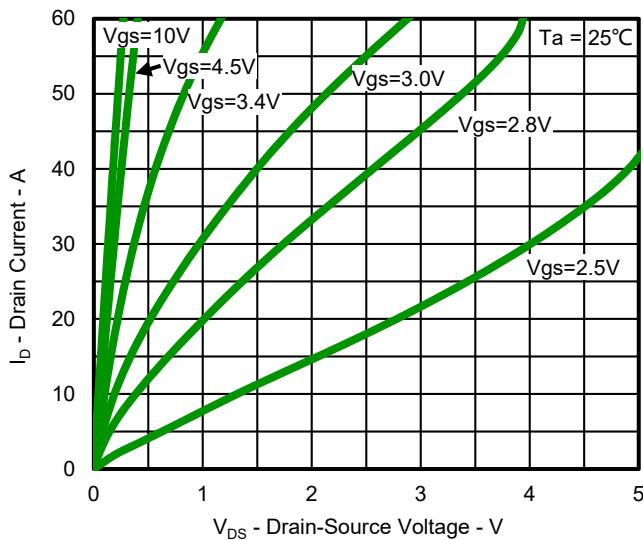


Fig.1 Output Characteristics

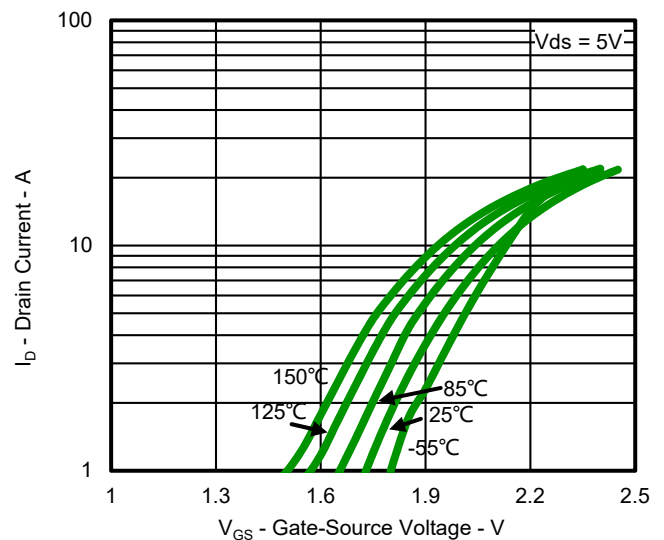


Fig.2 Typical Transfer Characteristic

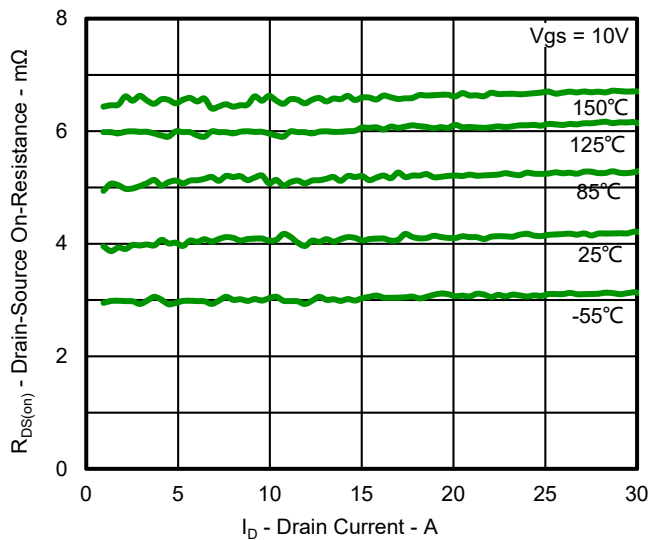


Fig.3 Typical On-Resistance vs Drain Current and Temperature

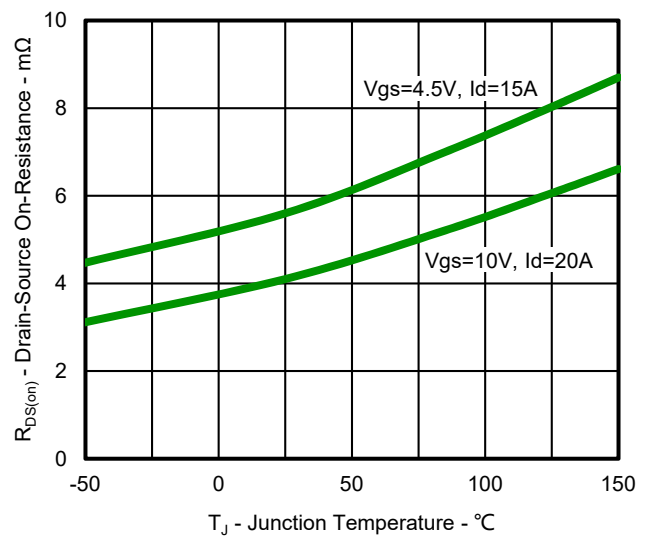


Fig.4 On-Resistance Variation with Temperature

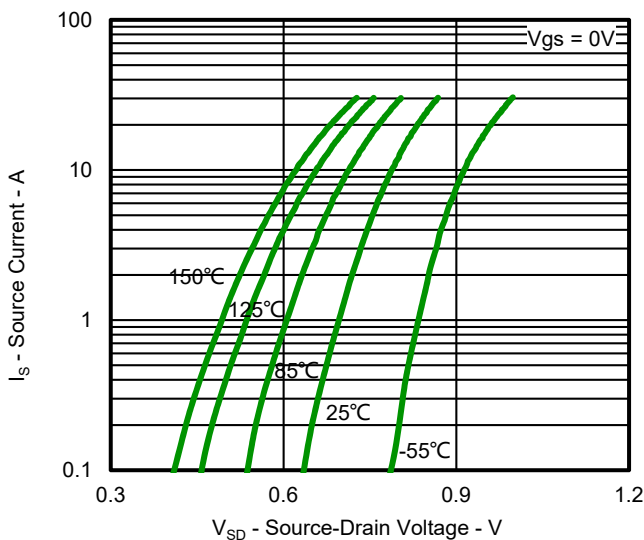


Fig.5 Diode Forward Voltage vs. Current

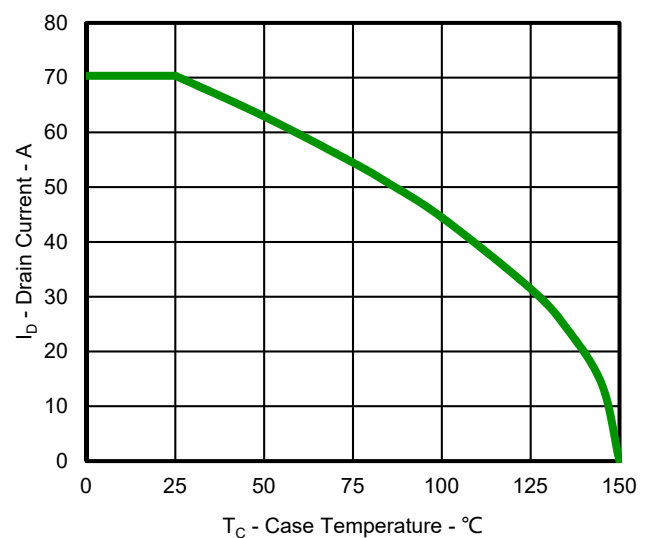


Fig.6 Maximum Drain Current vs. Case Temperature

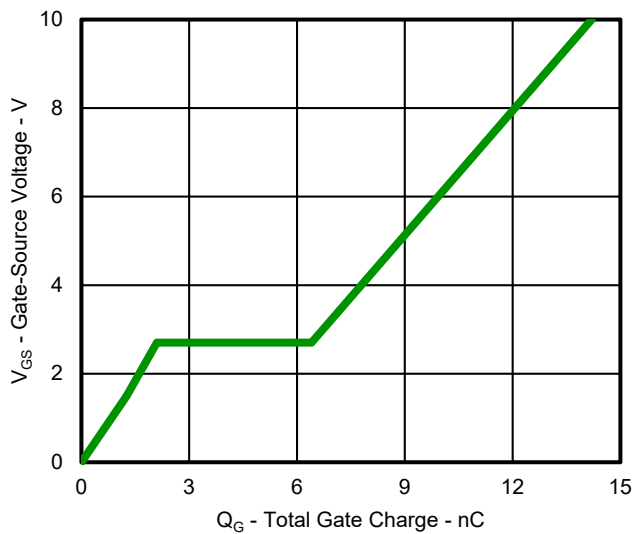


Fig.7 Gate Charge Characteristics

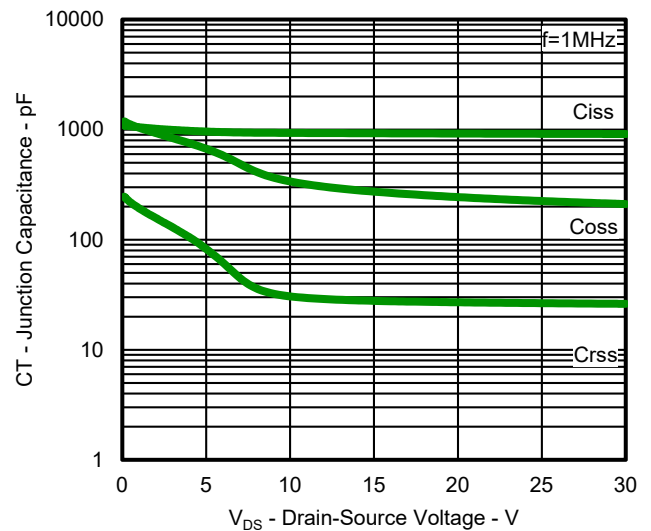


Fig.8 Typical Junction Capacitance

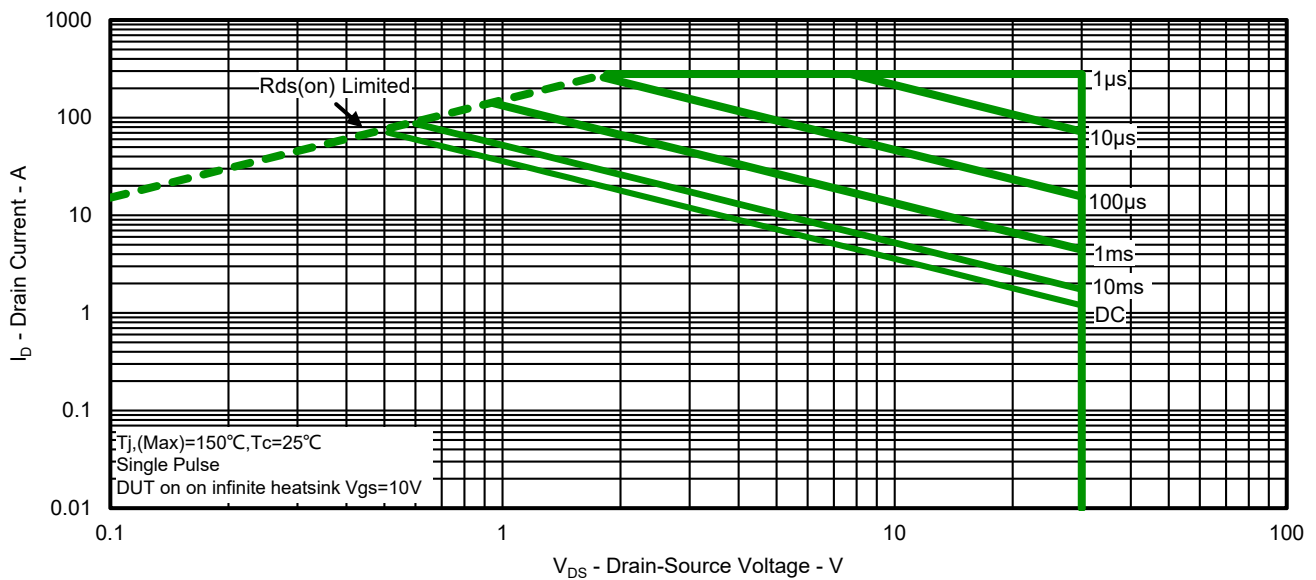


Fig.9 Safe Operation Area

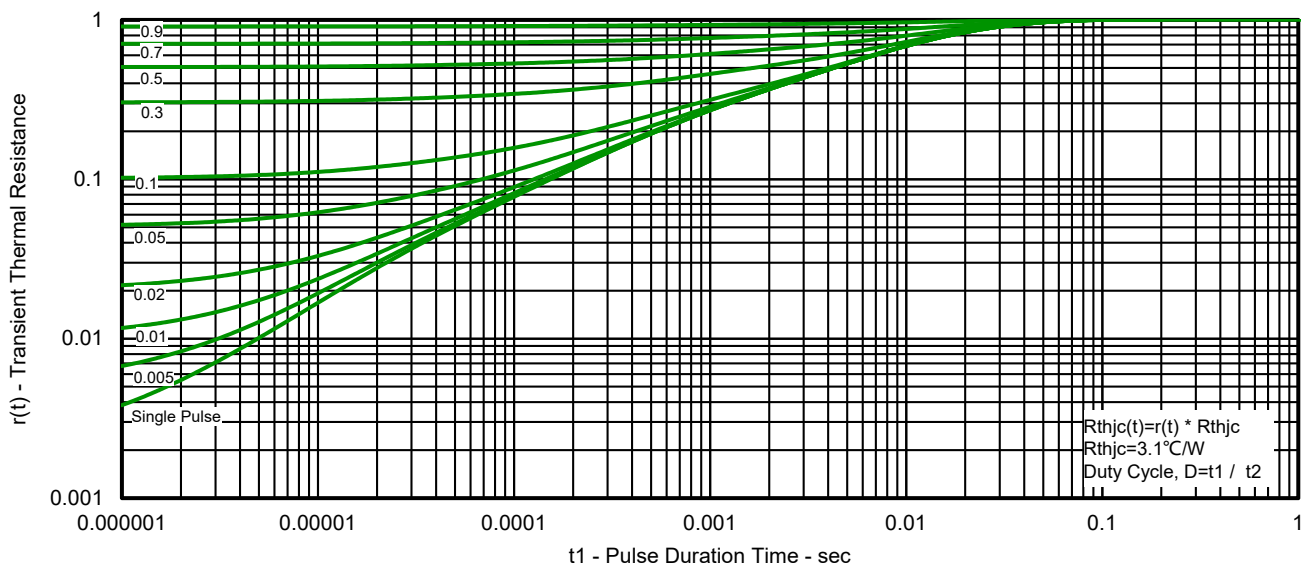
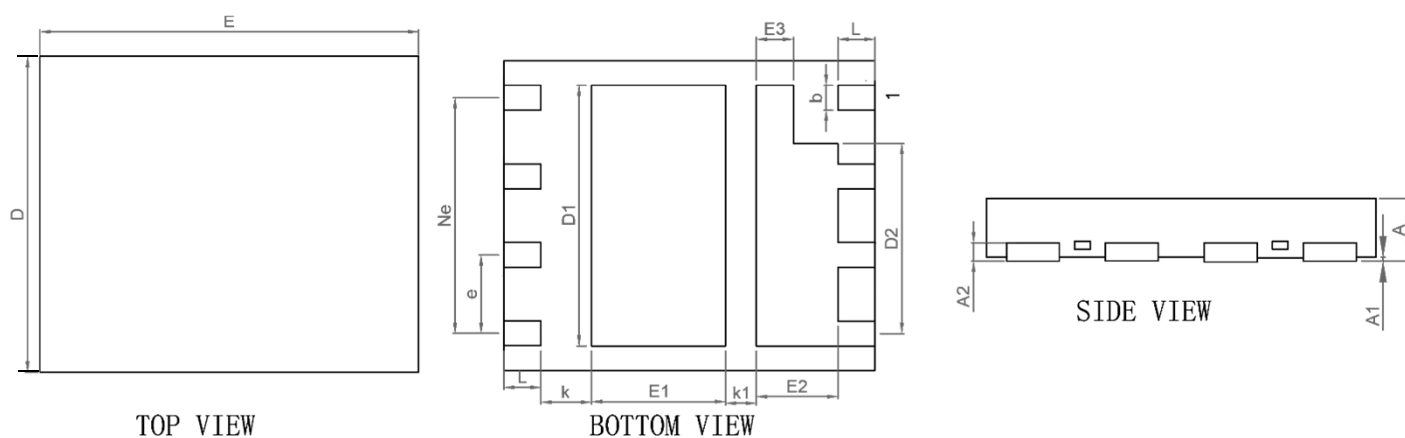


Fig.10 Transient Thermal Resistance

Product Dimension (DFN5060-8L)



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.36	0.46	0.014	0.018
A2	0.203 BSC		0.008 BSC	
D	4.90	5.10	0.193	0.201
D1	4.15	4.25	0.163	0.167
D2	2.87	3.27	0.113	0.129
E	5.90	6.10	0.232	0.240
E1	2.02	2.32	0.080	0.091
E2	1.22	1.42	0.048	0.056
E3	0.55	0.65	0.022	0.026
e	1.27 Ref		0.050 Ref	
Ne	3.81 BSC		0.150 BSC	
k	0.71	0.91	0.028	0.036
k1	0.40	0.60	0.016	0.024
L	0.55	0.65	0.022	0.026

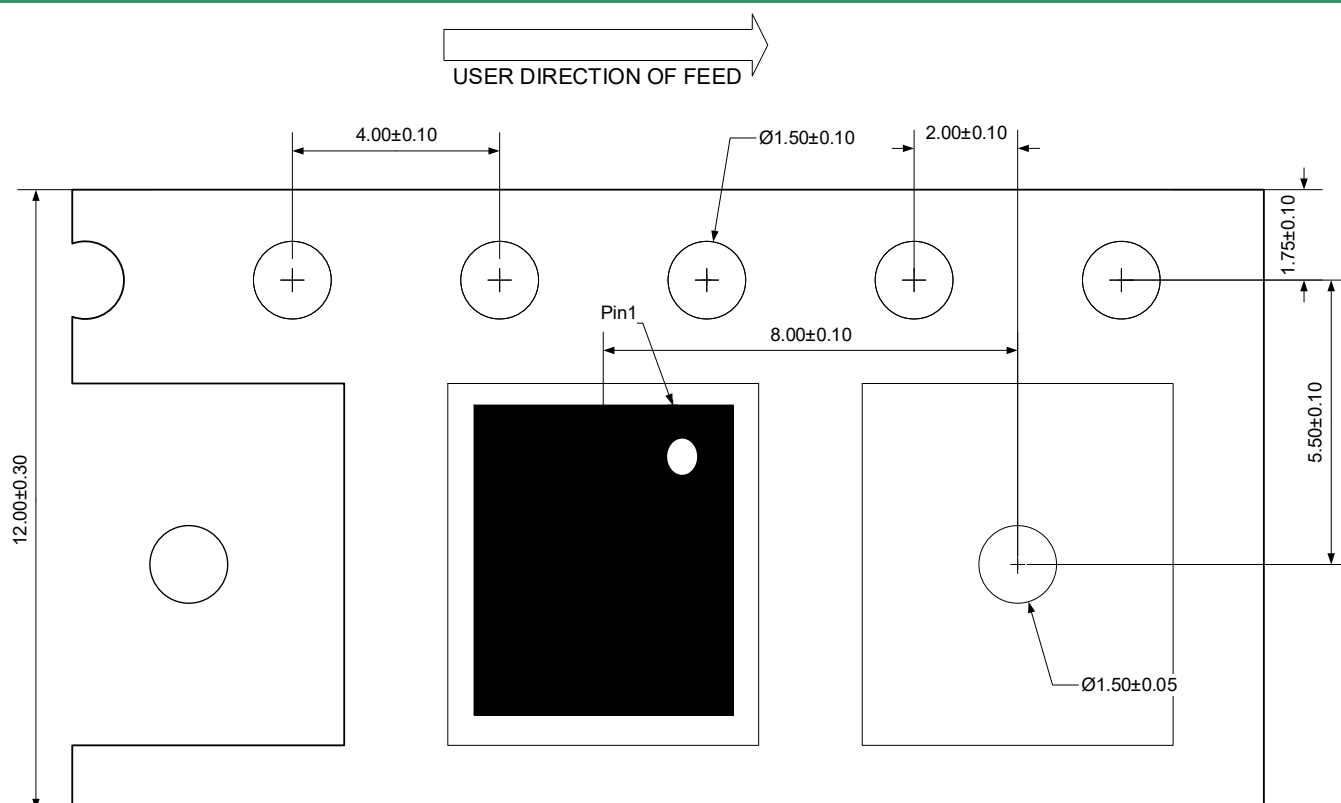
N-Channel MOSFET

PDSM8N03R5L

Ordering Information

Package	Reel	Shipping
DFN5060-8L	13"	5000 / Tape & Reel

Load With Information



Unit:mm

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