

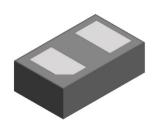


## **Uni-directional 6.3V High Capacitance ESD Protector**

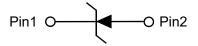
#### **Description**

The PESDHC2FD6V3UMF ESD protector is designed to replace multilayer varistors (MLVs) in portable applications such as cell phones, notebook computers, and PDA's. They feature large cross-sectional area junctions for conducting high transient currents, offer desirable electrical characteristics for board level protection, such as fast response time, lower operating voltage, lower clamping voltage and no device degradation when compared to MLVs. The PESDHC2FD6V3UMF protects sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD) and other voltage induced transient events.

The PESDHC2FD6V3UMF is available in a DFN1006-2L package with working voltages of 6.3 volt. It gives designer the flexibility to protect one unidirectional line in applications where arrays are not practical. Additionally, it may be "sprinkled" around the board in applications where board space is at a premium.



DFN1006-2L(Bottom View)

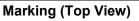


**Circuit Diagram** 

#### Feature

- 700W peak pulse power per line (t<sub>P</sub> = 8/20µs)
- DFN1006-2L package
- Response time is typically < 1 ns</p>
- Unidirectional configurations
- Low clamping voltage
- RoHS compliant
- Transient protection for data lines to IEC 61000-4-2(ESD) ±30kV(air), ± 30kV(contact); IEC 61000-4-5 (Lightning) 60A (8/20us)





#### **Applications**

- Cell phone handsets and accessories
- Personal digital assistants (PDA's)
- > Notebooks, desktops, and servers
- Portable instrumentation
- Cordless phones
- Digital cameras
- Peripherals

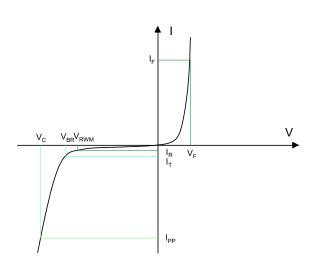
#### **Mechanical Characteristics**

- Mounting position: Any
- Qualified max reflow temperature:260°C
- Device meets MSL 1 requirements
- DFN1006-2L without plating

## PESDHC2FD6V3UMF

### **Electronics Parameter**

Symbol	Parameter		
V <sub>RWM</sub>	Peak Reverse Working Voltage		
I <sub>R</sub>	Reverse Leakage Current @ V <sub>RWM</sub>		
V <sub>BR</sub>	Breakdown Voltage @ I <sub>T</sub>		
Ι <sub>Τ</sub>	Test Current		
I <sub>PP</sub>	Maximum Reverse Peak Pulse Current		
V <sub>c</sub>	Clamping Voltage @ I <sub>PP</sub>		
P <sub>PP</sub>	Peak Pulse Power		
CJ	Junction Capacitance		
I <sub>F</sub>	Forward Current		
V <sub>F</sub>	Forward Voltage @ I <sub>F</sub>		



## Electrical characteristics per line@25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Тур.	Max.	Units
Peak Reverse Working Voltage	V <sub>RWM</sub>	-	-	-	6.3	V
Breakdown Voltage	$V_{BR}$	I <sub>t</sub> = 1mA	6.5	7.0	8.5	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> =6.3V	-	-	1	μA
Clamping Voltage <sup>1)</sup>	V <sub>c</sub>	TLP = 16A, t <sub>p</sub> = 100ns	-	7.0	-	V
Clamping Valtage <sup>2)</sup>	V <sub>c</sub>	I <sub>PP</sub> = 10A,t <sub>P</sub> = 8/20μs	-	8.0	10.0	V
Clamping Voltage <sup>2)</sup>		I <sub>PP</sub> = 60A,t <sub>P</sub> = 8/20µs	-	11.5	14.0	V
Junction Capacitance	C」	V <sub>R</sub> = 0V,f = 1MHz	-	160	200	pF

Notes:

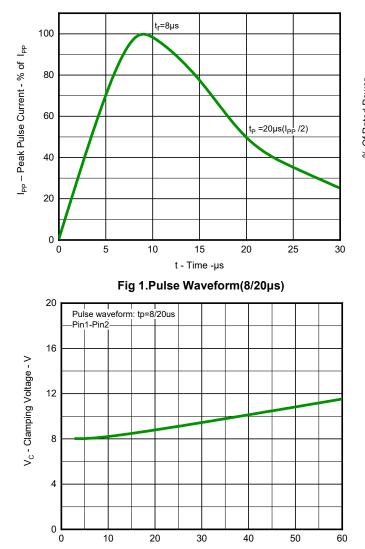
1.TLP parameter:  $Z_0=50\Omega$ ,  $t_p=100$  ns,  $t_r=2$  ns, averaging window from 60 ns to 80 ns.  $R_{DYN}$  is calculated from 4A to 16A. 2.Non-repetitive current pulse, according to IEC61000-4-5.

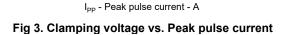
### Absolute maximum rating@25°C

Rating	Symbol	Value	Units
Peak Pulse Power ( t <sub>P</sub> = 8/20µs )	P <sub>PP</sub>	700	W
Peak Pulse Current ( t <sub>P</sub> = 8/20µs )	I <sub>PP</sub>	60	А
Lead Soldering Temperature	TL	260 (10 sec)	°C
Junction and Storage Temperature Range	T <sub>J,</sub> T <sub>STG</sub>	-55~+150	°C
ESD Protection-Contact Discharge	V <sub>ESD</sub>	±30	kV
ESD Protection-Air Discharge	V <sub>ESD</sub>	±30	kV

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### **Typical Characteristics**





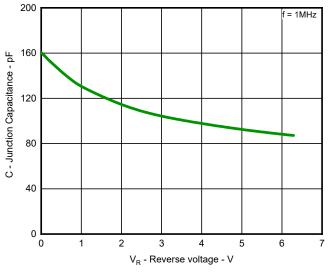
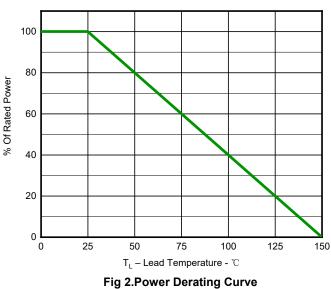


Fig 5. Capacitance vs. Reveres voltage



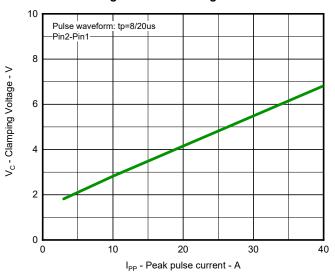


Fig 4. Clamping voltage vs. Peak pulse current

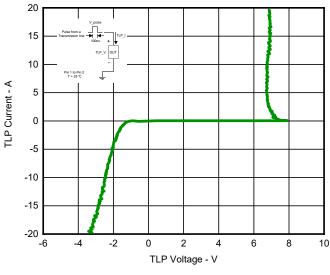


Fig 6. TLP Measurement

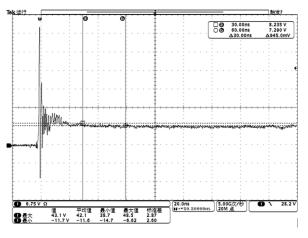


Fig 7. Clamping Voltage at IEC61000-4-2 +8kV Pulse Waveform

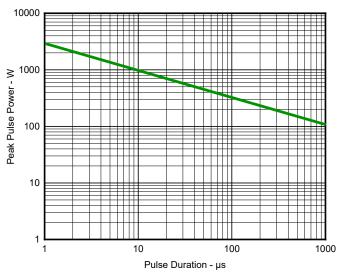
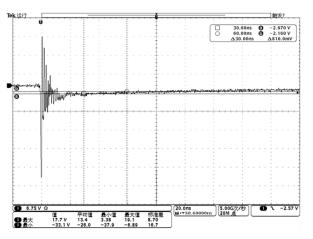


Fig 9. Non Repetitive Peak Pulse Power vs. Pulse time

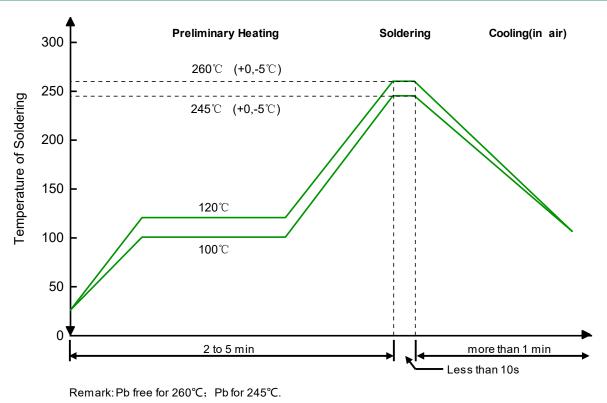
# PESDHC2FD6V3UMF





PESDHC2FD6V3UMF

#### **Solder Reflow Recommendation**



#### **PCB** Design

For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

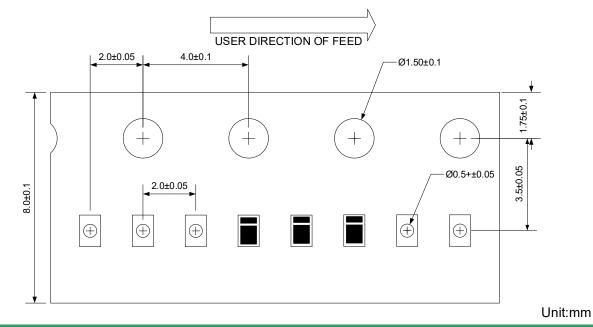
- > Do not use stubs, but place the cathode of the TVS diode directly on the signal trace.
- > Do not make false economies and save copper for the ground connection.
- > Place via holes to ground as close as possible to the anode of the TVS diode.
- > Use as many via holes as possible for the ground connection.
- > Keep the length of via holes in mind! The longer the more inductance they will have.

#### **Ordering information**

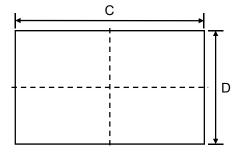
Device	Package	Reel	Shipping
PESDHC2FD6V3UMF	PESDHC2FD6V3UMF DFN1006-2L (Pb-Free)		10000 / Tape & Reel

# PESDHC2FD6V3UMF

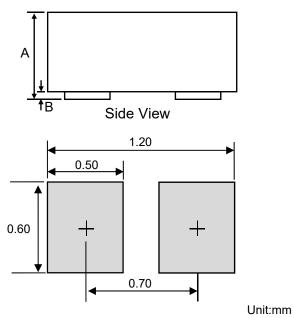
### Load with information

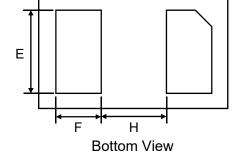


## Product dimension (DFN1006-2L)









Dim	Millimeters		Inches		
Dim	Min	Max	Min	Max	
А	0.34	0.498	0.013	0.020	
В	0.00	0.05	0.000	0.002	
С	0.95	1.08	0.037	0.043	
D	0.55	0.65	0.022	0.026	
E	0.40	0.60	0.016	0.024	
F	0.20	0.30	0.008	0.012	
Н	0.40 Typ.		0.015 Тур.		

Suggested PCB Layout

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