

## Description

The PSC5425A combines a highly integrated switch-mode charger, to minimize single-cell Lithium-ion (Li-ion) charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

The charging parameters and operating modes are programmable through an I<sup>2</sup>C interface. The charger and boost regulator circuits switch at selectable frequency to lower the EMI and minimize the size of external passive components.

The PSC5425A provides battery charging in three phases: conditioning, constant current, and constant voltage.

To ensure USB compliance and minimize charging time, the input current is limited to the value set through the I<sup>2</sup>C host. Charge termination current is programmable through the I<sup>2</sup>C host.

The integrated circuit (IC) automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode with leakage from the battery to the input prevented. Charge status is reported back to the host through the I<sup>2</sup>C port.

The PSC5425A can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery.

The PSC5425A is available in a 20-bump, 0.4mm pitch WLCSP package.

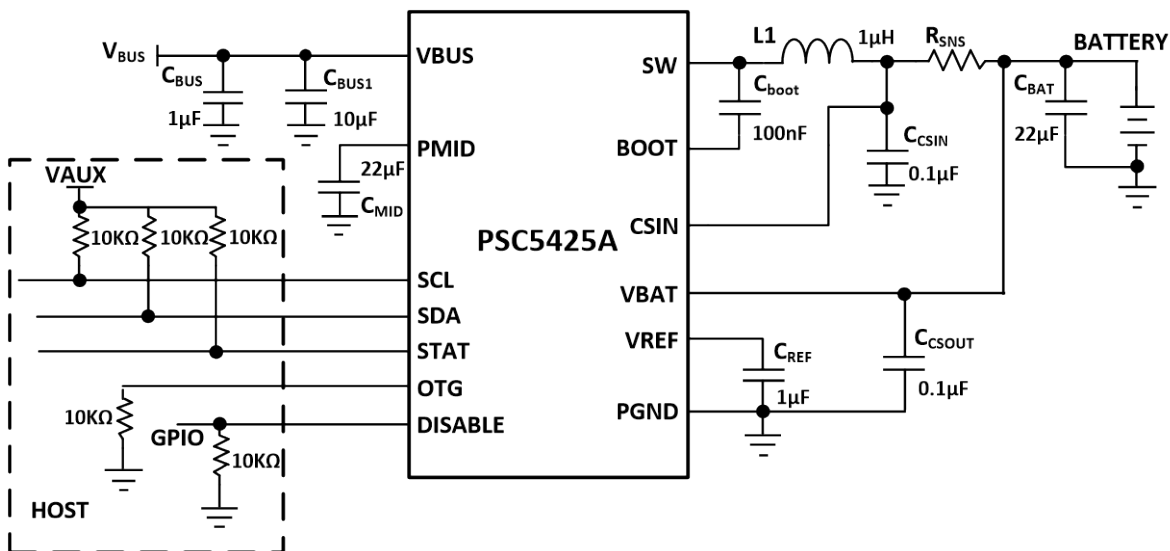


Figure 1: Typical Application

### Feature

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Faster Charging than Linear
- Charge Voltage Accuracy:  $\pm 0.5\%$  25°C
- $\pm 5\%$  Charge Current Regulation Accuracy
- 20V Absolute Maximum Input Voltage
- 6V Maximum Input Operating Voltage
- 2.25A Maximum Charge Rate

### Application

- Cellular Phones, Smart Phones, PDAs
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

**USB-Compliant Single-Cell Li-Ion Switching Charger with USB-OTG Boost Regulator**

- Programmable through I<sup>2</sup>C Interface:
  - Input Current
  - Fast-Charge/Termination Current
  - Charger Voltage
  - Termination Enable
- Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint 1μH External Inductor
- Weak Input Sources Accommodated by Reducing Charging Current to Maintain Minimum VBUS Voltage
- Low Reverse Leakage to Prevent Battery Drain to VBUS
- 5V, 1.5A Boost Mode for USB OTG for 3.0 to 4.5V Battery Input

**Recommended External Components**

Key Components	Recommended specification
L1	Inductor, 1.0-2.2uH, +-20%, Isat>3A
C <sub>MID</sub>	Capacitor, 22μF, +-10%, >6V
C <sub>REF</sub>	Capacitor, 1μF, +-10%, >6V
C <sub>BUS</sub>	Capacitor, 1.0μF, +-10%, >16V
C <sub>BUS1</sub> (EOS option)	Capacitor, 10μF, +-10%, >16V
C <sub>BOOT</sub>	Capacitor, 33~100nF, +-10%, >6V

**Block Diagram**

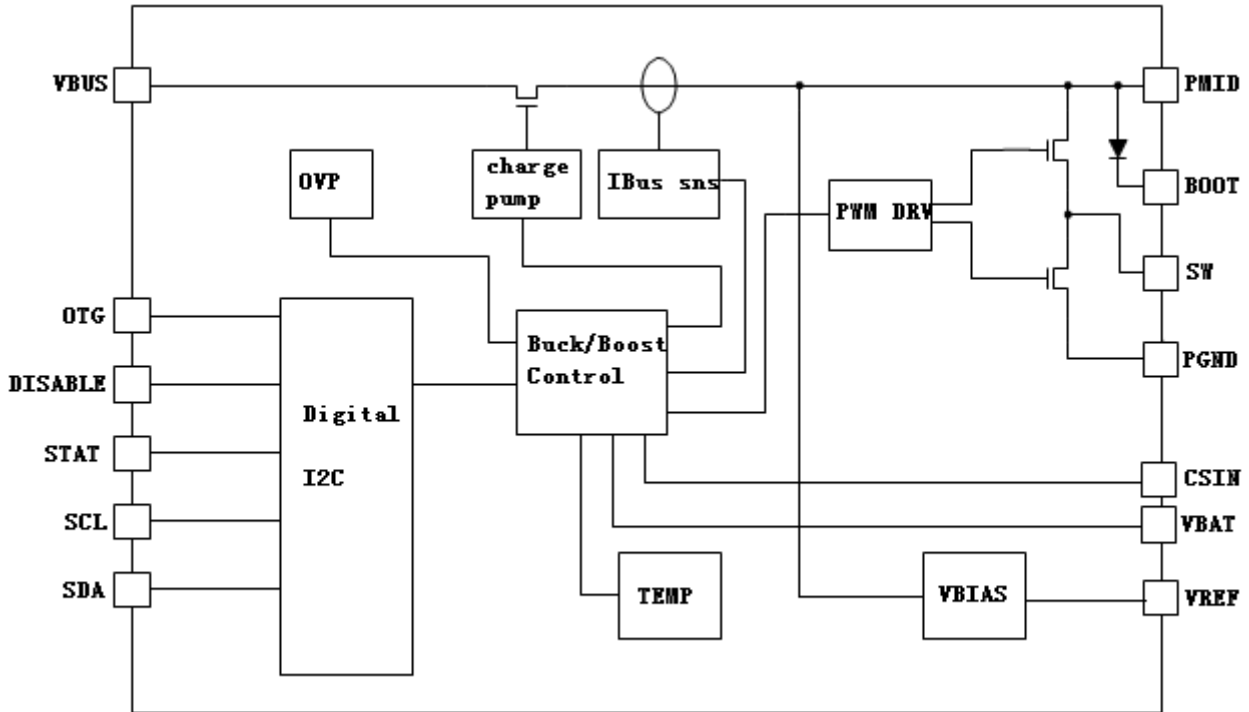


Figure 2: IC and System Block Diagram

**Pin Configuration**

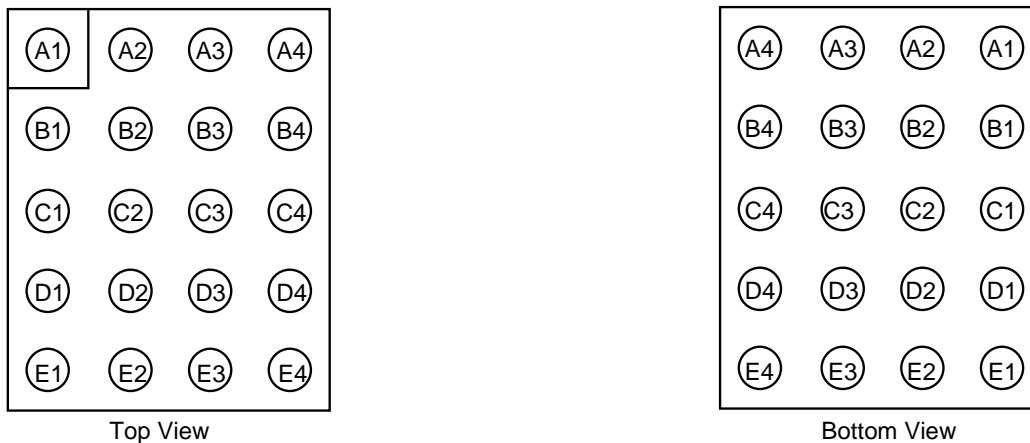


Figure 3: WLCSP-20 Pin Assignments

**Pin Definitions**

Pin#	Name	Description
A1,A2	VBUS	<b>Charger Input Voltage</b> and USB-OTG output voltage. Bypass with 1 $\mu$ F//10 $\mu$ F capacitor to PGND
A3	BOOT	<b>Boost strap capacitor</b> connection for high side NMOS gate driver. Connect 33nF~100nF ceramic capacitor (voltage rating $\geq$ 6V) from BOOT to SW pin.
A4	SCL	<b>I<sup>2</sup>C Interface Serial Clock</b> . This pin should not be left floating.
B1-B3	PMID	<b>Power Input Voltage</b> . Power input to the charger regulator, bypass point for the input current sense, and high-voltage input switch. Bypass with a minimum of 22 $\mu$ F, 6.3V capacitor to PGND.
B4	SDA	<b>I<sup>2</sup>C Interface Serial Data</b> . This pin should not be left floating.
C1-C3	SW	<b>Switching Node</b> . Connect to output inductor.
C4	STAT	<b>Status</b> . Open-drain output indicating charge status. The IC pulls this pin LOW when charge is in process.
D1-D3	PGND	<b>Power Ground</b> . Power return for gate drive and power transistors. The connection from this pin to the bottom of C <sub>MID</sub> should be as short as possible.
D4	OTG	<b>On-The-Go</b> . Enables boost regulator in conjunction with OTG_EN and OTG_PL bits (see Table 16).
E1	CSIN	<b>Current-Sense Input</b> . Connect to the sense resistor in series with the battery. The IC uses this node to sense current into the battery. Bypass this pin with a 0.1 $\mu$ F capacitor to PGND.
E2	DISABLE	<b>Charge Disable</b> . If this pin is "1", charging is disabled. When LOW, charging is controlled by I2C registers.
E3	VREF	<b>Bias voltage</b> . Connect to a 1 $\mu$ F capacitor to PGND. The output voltage is PMID, which is limited to 6.5V. Any resistor loading to VREF is <b>NOT</b> recommended.
E4	VBAT	<b>Battery Voltage</b> . Connect to the positive (+) terminal of the battery pack. Bypass with a 0.1 $\mu$ F capacitor to PGND if the battery is connected through long leads.

**Product dimension**

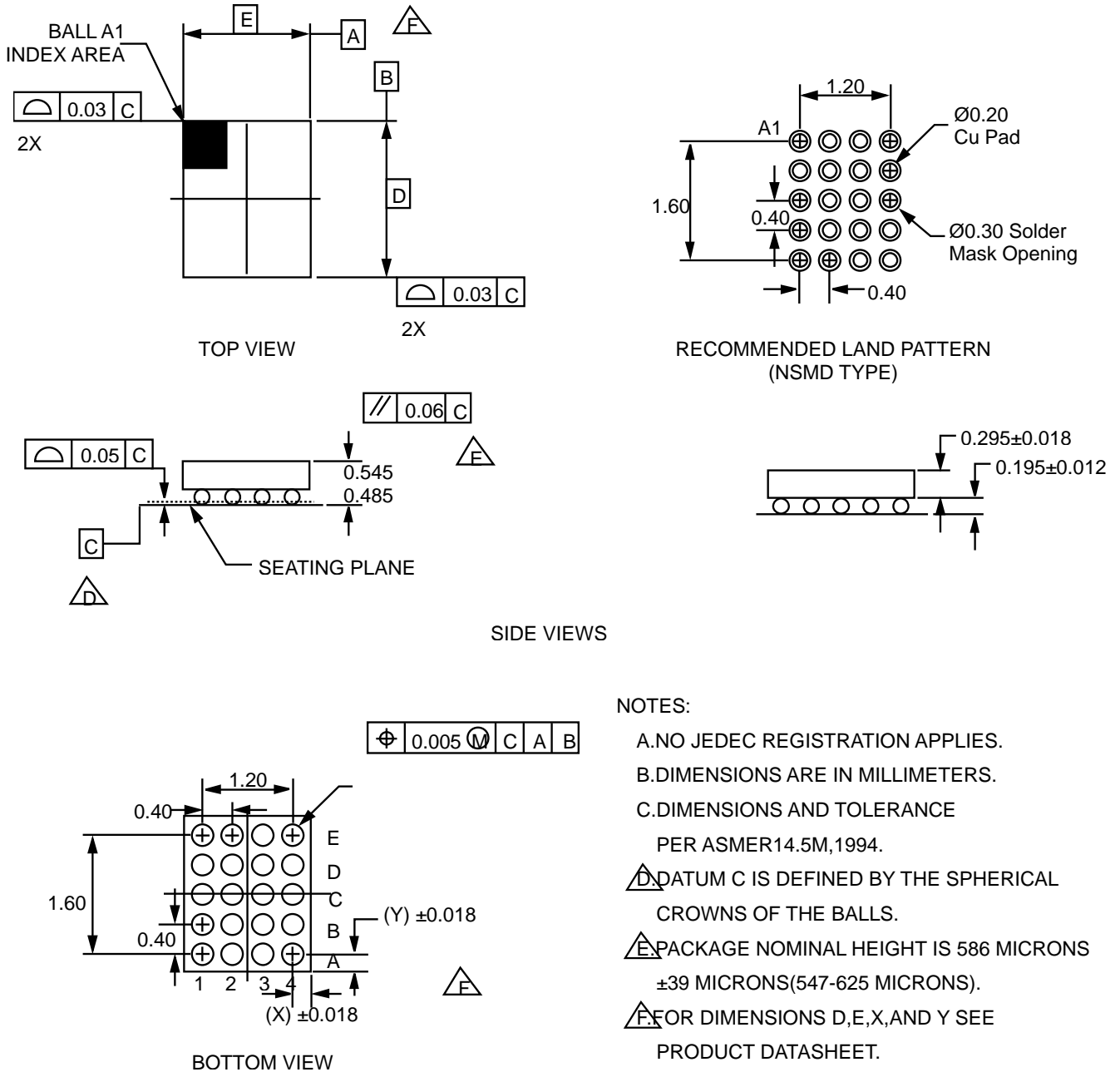



Figure 50. 20-Ball WLCSP, 4x5 Array, 0.4mm Pitch, 250µm Ball

**Product-Specific Dimensions (mm)**

Product	D	E	X	Y
PSC5425A	2.000±0.030	1.700±0.030	0.250	0.200


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